25 W Peak Power, Pulsed NIR LED Driver for DMS / OMS Applications

TND6416/D

INTRODUCTION

The Driver Monitoring System (DMS) is one of the key systems helping to improve both driver and passenger safety through detection of a driver's distraction, fatigue, or unresponsiveness. In recent years the demand for DMS has significantly increased because of new legislations, including both the European Union General Safety Regulations and the Safety Technology Roadmap published by the European New Car Assessment Program (Euro NCAP), for achieving a five−star safety rating. In a real−world there are a number of factors which need to be considered to make the driver monitoring system reliable. Common requirements are that the DMS needs to be functional considering factors such as:

- Lighting: 1 Lux during night−time to 100k Lux during daytime
- Eyewear: Clear glasses and sunglasses with >70% transmittance
- Facial Occlusion: Facemask, hats, long head hair fringe obscuring eyes

To assure a robust operation in different driving scenarios DMS systems incorporate a Near−Infrared (NIR) illumination. Operation at a narrow spectral band of around 940 nm is nowadays the most common design choice. There are several advantages of operation at 940 nm over other wavelengths such as 850 nm. 940 nm offers less interference from ambient sunlight and helps to significantly reduce the 'red glow effect', which is apparent at 850 nm. The main challenge when operating at 940 nm is the fact that the quantum efficiency of the image sensors drops when increasing the wavelength i.e. from 850 nm to 940 nm. Power LEDs are still the most common design choice for NIR illumination due to their good performance to price ratio, compared to other emerging technologies such as vertical−cavity surface−emitting laser (VCSEL). What is important to note is that 940 nm light is invisible to the human eye but can be harmful at higher power. Conformity with IEC 62471 for eye safety is vital for DMS operation. An LED driver with embedded eye−safety and diagnostics such as NCV7694 can significantly ease the design and bring benefits in terms of solution cost and PCB space compared to other less integrated NIR LED drivers without a dedicated eye−safety protection features.

There are various driver topologies used to power the NIR LEDs in DMS applications. Selection of the most suitable topology depends on particular Original Equipment Manufacturer (OEM) system requirements. A common approach is to power the LEDs from a pre−regulated voltage source such as Buck, Buck−Boost or Single−Ended Primary Inductance Converter (SEPIC) regulator and use a low−dropout current regulator as a second stage to keep the LED current constant across changing environmental conditions and LED manufacturing tolerances. Such a topology has been considered in this reference design. In terms of location of NIR illumination in the system, again, the location depends on the specific OEM requirements, but it is common to have it either embedded in the DMS Camera unit or implemented as a standalone unit separate from the camera unit.

A common method of driving the NIR LEDs in DMS systems is to produce short duration, high current pulses with high near−infrared light energy content. Such method helps to overcome the challenges associated with the external lighting environment, use of eyewear etc.

The timing chart in Figure 1 demonstrates the typical timing relationships between the NIR illumination and global shutter image sensor in the DMS system. For optimal performance NIR LEDs are synchronized with the image sensor frame exposure time. This is done with the help of a dedicated FLASH strobe control signal from the image sensor SoC. LEDs are being activated only for a fraction of the entire frame time to save power. In the example shown on Figure 1 the LED turn−on duty cycle is 3%. NIR illumination in such system needs to be able to deliver short bursts with large optical power but the average output power is relatively low. The reference design example described in this paper is based on 2x SFH 4725AS Power LEDs driven with 4 A, 500 μs bursts at 60 fps. As a result, the design can deliver 25 W power bursts with 0.74 W average power.

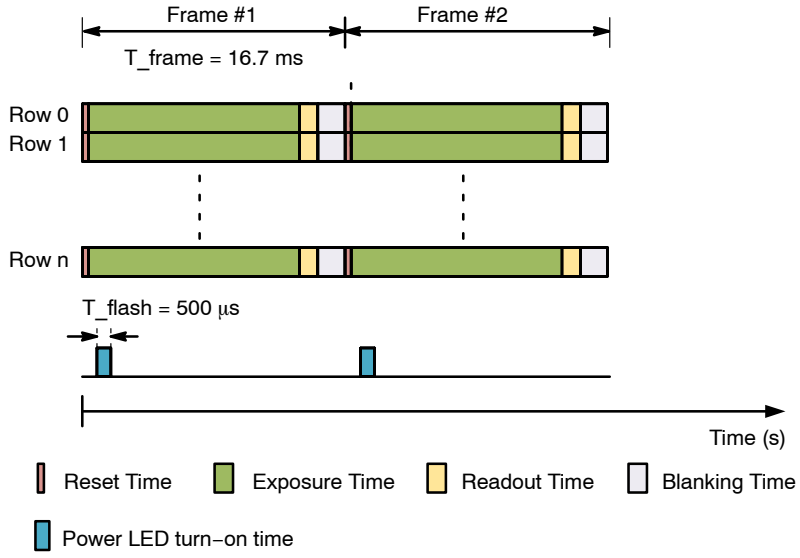

Figure 1. Timing Relationship between the NIR Illumination and Image Sensor in DMS

Figure 2 shows a block diagram of a DMS application with NIR illumination and DMS camera integrated into one unit and powered through Power−Over−Coax (POC). With POC, the image data captured by the image sensor, I^2C data, diagnostic data and power are transferred together using a single coaxial cable. This method helps to reduce cabling cost and weight. Separation of power and data on the ECU and Camera side is done by passive filter networks used within the power path and decoupling capacitor network used within the data path. With the POC approach the maximum current that can be delivered to the Camera from the ECU is limited. Typically, the coaxial cables used in POC have a loop resistance of ~2.3 Ω per meter that is why larger currents would incur large losses in the cable. Additionally, the current ratings of the POC inductors are usually limited to less than 1 A – i.e. larger currents would cause their magnetic saturation.

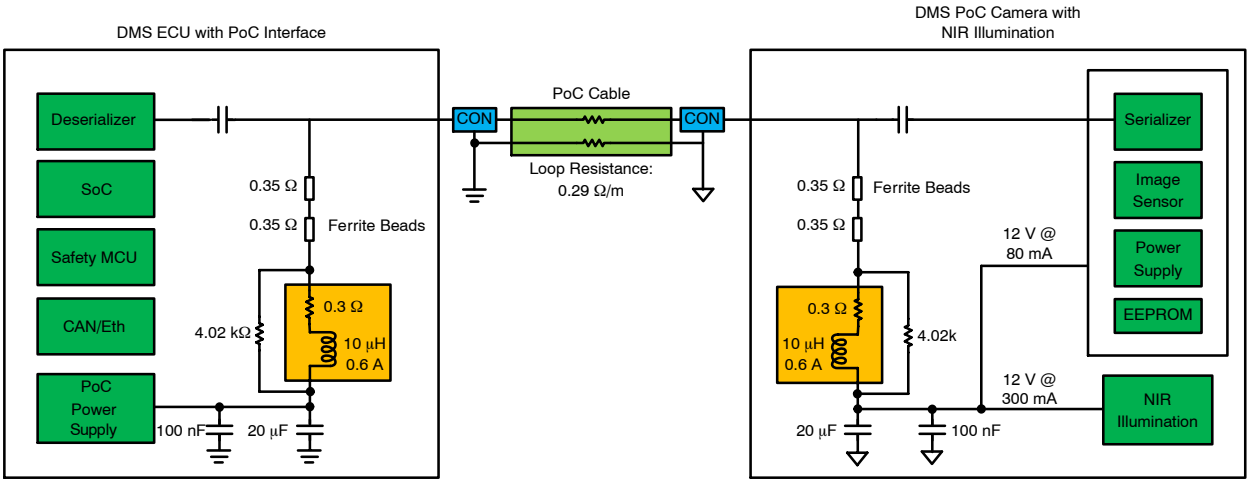

Figure 2. PoC DMS Camera with an Integrated NIR LED Driver

To protect the coaxial cable and POC filter components from an excessive current drawn, during the NIR LED current pulses, the POC powered NIR illumination shall incorporate a current limit circuit which limits the POC current to a safe level, as well as a local energy buffer able to support large LED current pulses. This reference design will demonstrate how to design such system in more detail.

NCV7694 REFERENCE DESIGN OVERVIEW

Figure 3 shows a 3D rendered picture of the reference design PCB. It also highlights the main components used in the design as well as describes the external connections.

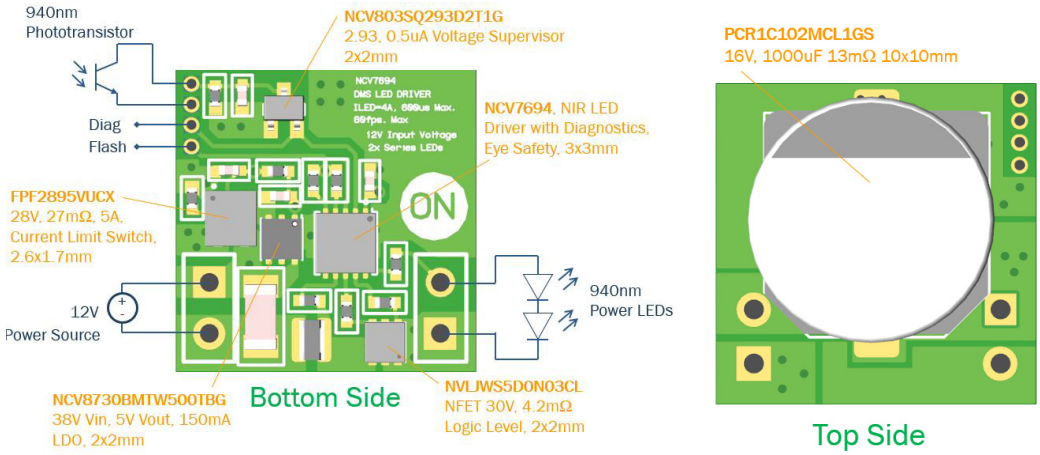

Figure 3. Overview of NCV7694 Reference Design PCB

Table 1 summarizes specifications of the reference design:

Table 1. SPECIFICATIONS OF THE NCV7694 REFERENCE DESIGN

POC Voltage Specification	12 V ±5%
Imager Frame Rate	30–60 fps
Pulsed Output (LED) Current	4 A
Input Current Limitation	500 mA typ.
Number of Series LEDs	2
LED Current Pulse Duration	Up to 500 μs
LED Wavelength	940 nm
Driver Proximity Sensing	30 cm typ.
Ambient Temperature	−40°C to +85°C
Diagnostics and Protection Features	Open of the LED String Short of the LED String Maximum LED current pulse width limited to 572 μs Maximum LED Current pulse frequency limited to 74 fps
Flash Signal Level	1.8 V logic compatible input
Diagnostics Output	5 V logic output
Initial Start Up Time	28 ms Typ.
Compatible Power LEDs	Evaluation performed with Osram SFH 4725AS
PCB Size	15 x 15 mm

DESCRIPTION OF THE SELECTED NIR LED DRIVER TOPOLOGY

The reference design assumes the use of two SFH 4725AS NIR Power LEDs, each driven with 4 A, 500 μs current pulses at frequency of 60 Hz (60 fps). It is assumed that such configuration can provide a sufficient NIR light illumination level, to assure the correct operation of the image processing algorithms.

Furthermore, it is assumed that a 12 V ±5% power supply, with a maximum nominal current carrying capability of 500 mA, is available in the system.

Figure 4 shows a block diagram of the LED driver topology used in the reference design. V_S is a 12 V ±5% constant voltage power supply. I_{LIM} is a low−dropout constant current limiter, to keep the maximum current drawn from the power supply to 500 mA, as it is assumed that 12 V is supplied through POC. D1 and D2 are the two SFH 4725AS LEDs connected in series. The NCV7694 controller is used to drive an external NMOS to regulate the current through the LEDs to 4 A, as soon as the FLASH signal is activated. R_{SNS} is a power resistor used to measure the LED current. The voltage developed across R_{SNS} is used by NCV7694 to control the gate of the external MOSFET T2. Due to the 500 mA input current limitation, the required 4 A LED current pulses cannot be directly drawn from the 12 V power supply. Due to this fact a hold−up capacitor C_{BULK} is required to store enough energy to drive the LEDs with 4 A during the 500 μs LED flash duration.

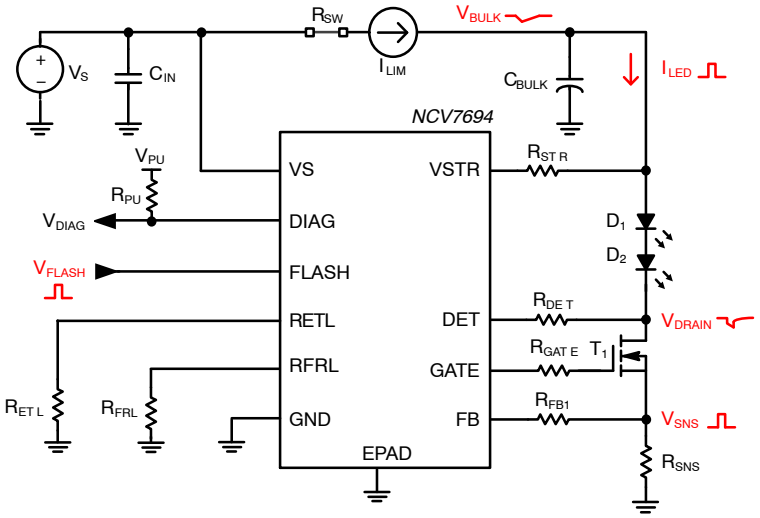

Figure 4. NCV7694 Based LED Driver Operating Principle

STEP−BY−STEP DESIGN GUIDE

Verification of the Maximum Supported LED Turn−on Time

As the first design step, it is recommended to check if the topology shown on Figure 4 can meet the target LED pulse current duration, given the required frame rate, LED current and the limitations of the power supply current. Such verification can be made according to the Equation 1:

$$T_{ON(MAX)} = \frac{1}{\text{frame rate}} \cdot \frac{I_{LIM}}{I_{LED}} \quad \text{(eq. 1)}$$

where:

$T_{ON(MAX)}$ − Maximum supported LED pulse current duration (s)

Frame rate − Target image sensor frame rate (fps)

I_{LIM} − Input Current limit value (A)

I_{LED} − LED current (A)

Considering the design input parameters summarized in Table 1 i.e. frame rate = 60 fps, I_{LIM} = 0.5 A, I_{LED} = 4 A, the maximum supported LED pulse current duration is $T_{ON(MAX)}$ = 2.08 ms.

Based on this initial check it can be expected that the topology shown in Figure 4 is a good candidate for this design and the needed T_{ON} = 500 μs can be met. This initial check doesn't consider thermal aspects which will be analyzed later in this document.

In case the required T_{ON} exceeds the calculated $T_{ON(MAX)}$, a potential solution is to increase the power supply voltage and introduce a voltage pre−regulator stage to effectively reduce the current drawn from the power supply as shown on Figure 5.

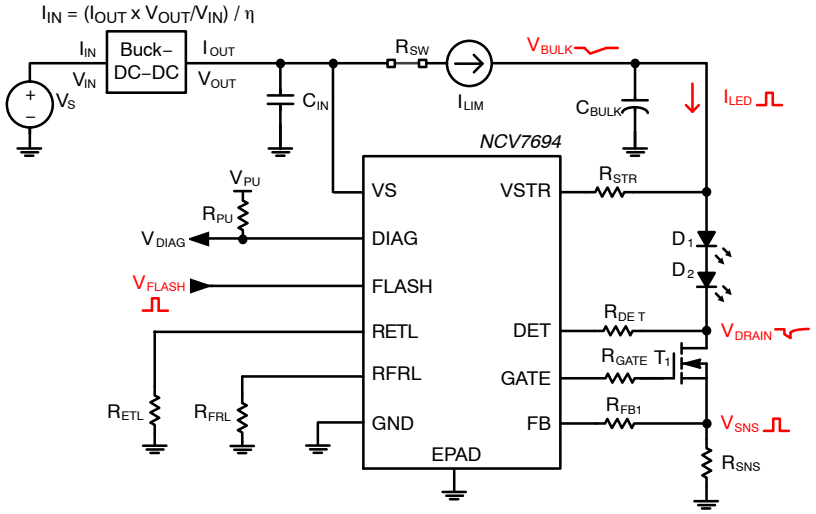

Figure 5. NCV7694 Based LED Driver with an Additional Buck DC−DC Stage

Hold−up Capacitor Selection

The next step is to calculate the required hold−up capacitor value C_{BULK}. It needs to be sufficiently large to maintain enough voltage across D1, D2, T1 and R_{SNS} for the LED current to be constant during the entire on−time period. The minimum required voltage headroom should be determined based on D1, D2 and T1 device specifications. Based on the SFH 4725AS datasheet the maximum forward voltage V_F of this LED is 4.1 V at I_{LED} = 4 A across temperature of −40°C to 145°C and process variations. In case of T1 it is desired to keep its drain−source voltage drop, V_{DS}, as low as possible to minimize the power losses within the MOSFET but high enough to operate this device in saturation. In this example V_{DS} = 0.5 V was picked for calculations. The sensing voltage V_{SNS} voltage is kept constant at 0.3 V by the NCV7694 feedback loop.

Based on these inputs it is possible to use Equation 2 to determine the required minimum hold−up capacitance:

$$C_{BULK(MIN)} > \frac{I_{LED} - I_{LIM}}{V_{BULK(MIN)} - 2 \cdot V_{LED(MAX)} - V_{DS} - V_{SNS}} \cdot T_{ON} \quad \text{(eq. 2)}$$

where:

$C_{BULK(MIN)}$− Minimum hold−up capacitance (F)

I_{LED} − NIR LED current (A)

$V_{LED(MAX)}$ − Maximum diode VF voltage (V)

I_{LIM} − Input current limit (A)

V_{DS}− MOSFET voltage drop Vds (V)

V_{SNS} − Sensing voltage (V)

T_{ON} − LED on−time (s)

$V_{BULK(MIN)}$ − Minimum power supply input voltage (V)

Design specification:

$V_{BULK(MIN)}$ = 11.4 V, $V_{LED(MAX)}$ = 4.1 V, V_{DS} = 0.5 V, V_{SNS} = 0.3 V, I_{LED} = 4.0 A, I_{LIM} = 500.0 mA, T_{ON} = 500 μs

Substituting these to Equation 2 gives the following result:

$$C_{BULK(MIN)} > \frac{4.0\ A - 0.5\ A}{11.4\ V - 2 \cdot 4.1\ V - 0.5\ V - 0.3\ V} \cdot 500\ \mu s = 730\ \mu F$$

When selecting a hold−up capacitor, it is important to select a part with low ESR and sufficient ripple current capability. In the design Nichicon PCR1C102MCL1GS, a 1000 μF, 16 V aluminum polymer capacitor with an ESR of 13 mΩ and a ripple current of 4.3 A has been selected. Since the hold−up capacitor has a significant impact on the overall solution size, at this point it is good to verify if the design based on the selected capacitor will be able to meet the required PCB dimensions.

MOSFET Selection

Proper selection of the MOSFET is essential in case of the LED driver reference design. The average power dissipation in the MOSFET can be estimated using Equation 3:

$$P_{D\_T1(AVG)} = \left(\left(V_{BULK(MAX)} - \frac{\Delta V_{BULK(MIN)}}{2} \right) - 2 \cdot V_{LED(MIN)} - V_{SNS} \right) \cdot I_{LED} \cdot T_{ON} \cdot \text{frame rate} \quad \text{(eq. 3)}$$

where:

$P_{D\_T1(AVG)}$ − Average MOSFET power dissipation (W)

$V_{BULK(MAX)}$ − Maximum bulk capacitor voltage (V)

$\Delta V_{BULK(MIN)}$ − Minimum bulk capacitor voltage dip during LED on−time (V)

$V_{LED(MIN)}$ − Minimum LED forward voltage drop (V)

V_{SNS} − Current shunt voltage (V)

I_{LED} − LED current (A)

T_{ON} − LED turn−on time (s)

Frame rate − image sensor frame rate (fps)

$\Delta V_{BULK(MIN)}$ in Equation 3 can be calculated using the following formula:

$$\Delta V_{BULK(MIN)} = \frac{T_{on} \cdot (I_{LED} - I_{LIM})}{C_{BULK(MAX)}} \quad \text{(eq. 4)}$$

where:

$\Delta V_{BULK(MIN)}$ = Minimum bulk capacitor voltage dip during LED on−time (V)

T_{ON} − LED turn−on time (s)

I_{LED} − LED current (A)

I_{LIM} − Input current limit value (A)

$C_{BULK(MIN)}$ − Maximum hold−up capacitance (F)

Considering the reference design requirements, Equation 3 yields the following results:

$$P_{D\_T1(AVG)} = ((12.6\ V - 1.46\ V) - 2 \cdot 2.63\ V - 0.3\ V) \cdot 4\ A \cdot 0.5\ ms \cdot 60\ fps = 706\ mW$$

The power dissipation calculated above can be used to estimate the MOSFET self−heating for a given PCB size through a computational fluid dynamics (CFD) type of simulation.

To minimize the PCB size, the NVLJWS5D0N03CL MOSFET in PWR22 2 x 2 mm package was selected. In the case of this reference design it was estimated that the overall MOSFET junction to ambient thermal resistance (Θ_{JA}) is ~61°C/W. The thermal resistance Θ_{JA} leads to self−heating of the MOSFET ΔT_J of about 43°C, which results in a junction temperature T_J of 128°C at an ambient temperature $T_{A(MAX)}$ of 85°C. This leaves 47°C of headroom with respect to NVLJWS5D0N03CL maximum operating junction temperature T_J of 175°C.

The self heating ΔT_J of 43°C is the average junction temperature increase as it is based on the average MOSFET power dissipation and steady state Θ_{JA}. To find the peak T_J, a SPICE simulations according to Figure 6 was performed.

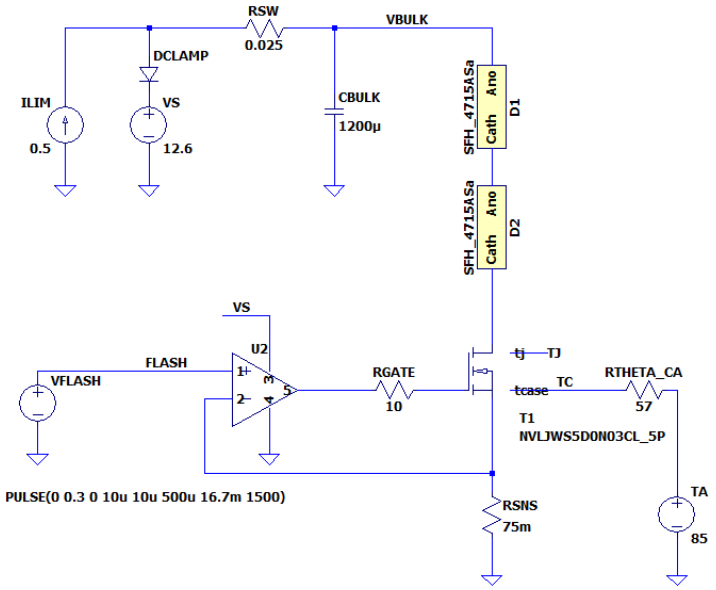

Figure 6. NVLJWS5D0N03CL Junction Temperature Simulation Setup

Figure 7 shows the junction temperature simulation results. After 10 seconds the junction temperature reaches a steady state. During this time the average junction temperature T_J increases from initially 85°C to 128°C, which matches with the value predicted by calculations.

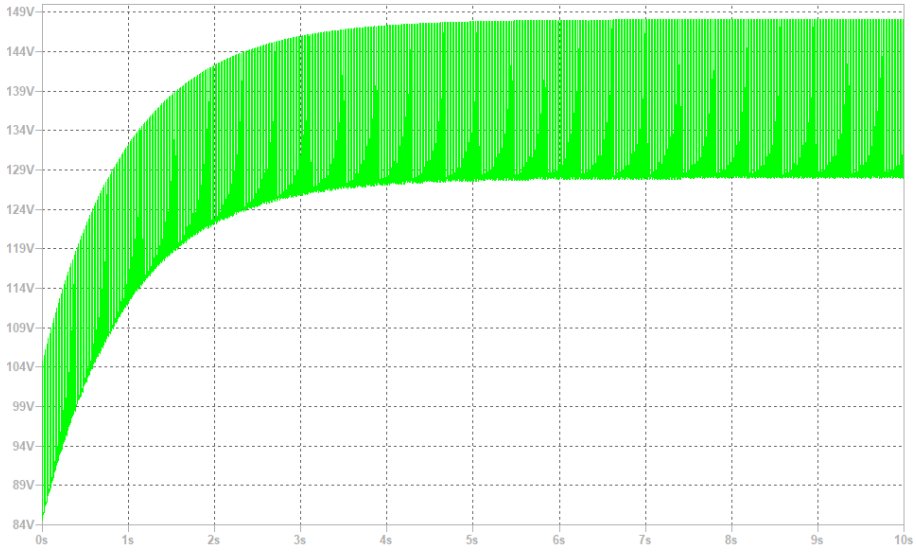

Figure 7. Simulated NVLJWS5D0N03CL Junction Temperature

Figure 8 shows the simulated MOSFET junction temperature during a drain current pulse in greater detail. As a result of large instantaneous power dissipation during the drain current pulse, the junction temperature T_J increases by about 20°C during this period above the steady−state value of 148°C peak.

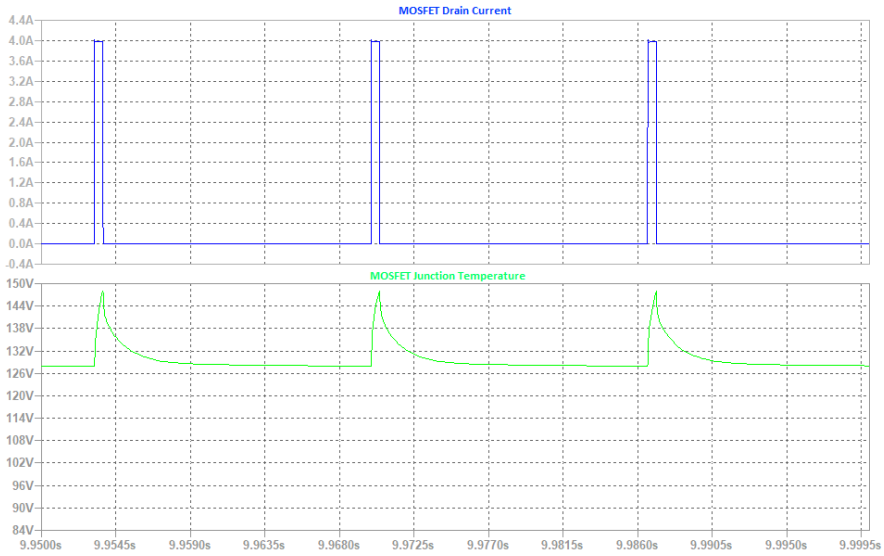

Figure 8. Detailed View of the Simulated MOSFET Junction Temperature and Drain Current

$T_{J(PEAK)}$ = 148°C is well below the maximum operating $T_{J(MAX)}$ of NVLJWS5D0N03CL of 175°C.

Since in this type of application the MOSFET is operated in saturation, an important part of the NVLJWS5D0N03CL analysis is the thermal stability evaluation. Low−voltage trench MOSFETs operated in saturation may potentially suffer from thermal instability which, in the worst case, could lead to MOSFET damage. The thermal instability effect, also know as the Spirito effect, is described in more details in [1].

To validate that the usage of NVLJWS5D0N03CL is safe in this regard, a thermal stability evaluation has been performed based on the following assumptions:

- MOSFET drain source voltage V_{DS} of 6 V
- Drain current pulse width of 1 ms
- MOSFET I_D was swept from 0 A until the device failed
- Device mounted on a tiny snap out card with 1 layer with 1 oz copper
- Testing performed on 5 units
- Initial junction temperature of $T_{J(initial)}$ of 128°C

Under the conditions anticipated above, according to measurements on 5 samples of NVLJWS5D0N03CL the device is not damaged until a drain current of 14 A is reached. This gives a very high confidence that the device can be safely used in the end application and won't suffer from thermal instability.

Design of Eye−safety Protection

The reference design features the following eye−safety protection mechanisms:

- Maximum LED on−time limitation
- Maximum LED turn−on frequency limitation
- Minimum permissible illumination distance.

NCV7694 allows to limit both maximum LED turn−on time and frequency.

Resistor R_{ETL} is used to set the maximum LED turn−on time according to the following equation:

$$T_{ON(MAX)} = \frac{R_{ETL}}{K_{ETL}} \quad \text{(eq. 5)}$$

where:

$T_{ON(MAX)}$ − maximum LED turn−on time limit (ms)

K_{ETL} − 2.5 ±13% across temperature and process (kΩ/ms)

R_{ETL} − value of the resistor connected to pin R_{ETL} of NCV7694 (kΩ)

As soon as the FLASH input is asserted NCV7694 starts to internally generate a voltage ramp at R_{ETL} pin with a slope which is inversely proportional to the R_{ETL} value. As soon as the R_{ETL} pin voltage reaches 1 V, the gate output is turned off, which disables MOSFET T1. Operation of this feature is explained on the timing diagram shown in Figure 10. Additionally, when the NCV7694 gate output goes low the /DIAG output is asserted which turns−off the FPF2895V high−side switch in series with the LEDs as shown on Figure 9. In case of this reference design R_{ETL} = 1.43 kΩ was chosen to limit T_{ON} to 572 μs. The R_{ETL} resistor allows to adjust T_{ON} from 320 μs up to 6 ms.

The frame rate limitation operates as follows: When the FLASH signal goes low, the voltage at NCV7694 R_{FRL} pin starts to rise. Before asserting of the next FLASH signal, the R_{FRL} pin voltage is compared with an internal reference voltage. If the R_{FRL} pin voltage is higher than the reference voltage, then T1 is turned−on. If that is not the case, then the NCV7694 /DIAG output becomes activated and the NCV7694 gate output turn−on is delayed until the R_{FRL} pin voltage exceeds the internal reference voltage. The formula below allows to calculate the minimum time between the

LED current pulses. The minimum supported off−time $T_{OFF(MIN)}$ is 8 ms which is corresponding to 125 Hz.

$$T_{OFF(MIN)} = \frac{R_{FRL}}{K_{FRL}} \quad \text{(eq. 6)}$$

where:

$T_{OFF(MIN)}$ − minimum off−time between the LED activations (ms)

K_{FRL} − 0.1 ±13% across temperature and process (kΩ/ms)

R_{FRL} − value of the resistor connected to pin R_{FRL} of NCV7694 (kΩ)

In the design R_{FRL} = 1.3 kΩ was used to limit the minimum time between the LED current pulses to 13 ms. This value corresponds to a maximum frame rate of 74 fps.

The minimum permissible distance between the source of NIR illumination and driver eyes is limited by an external phototransistor and NCV803 voltage detector, connected as depicted on Figure 9.

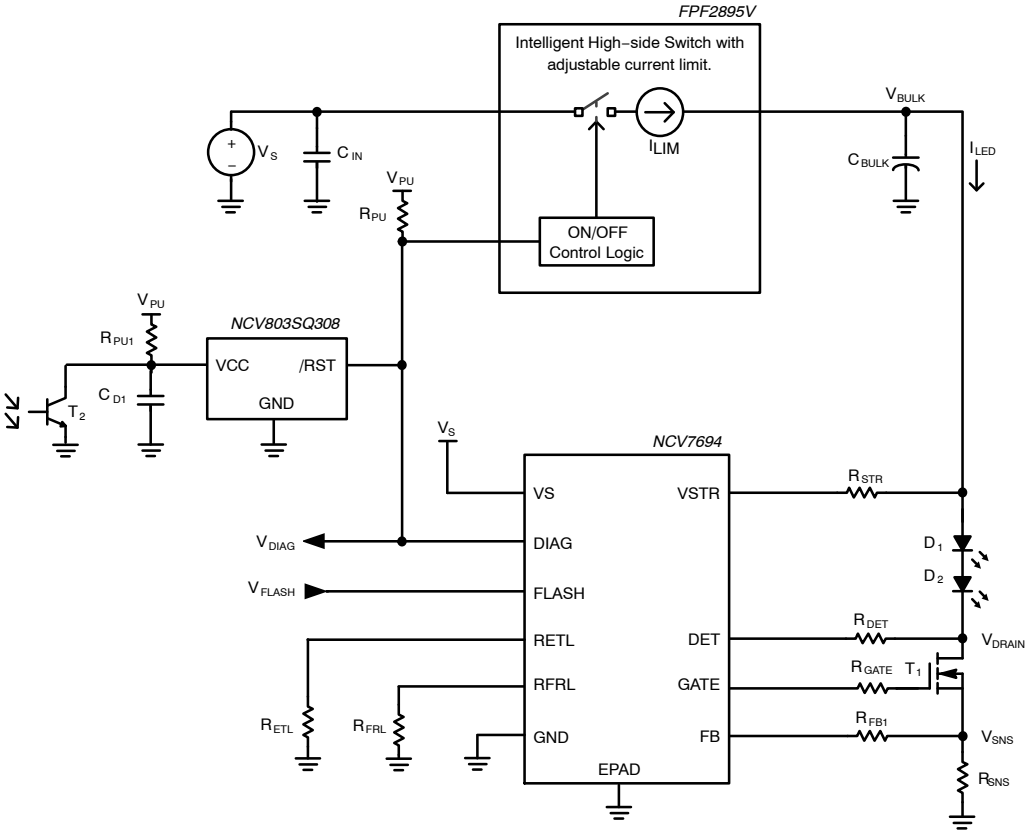

Figure 9. LED Driver Block Diagram

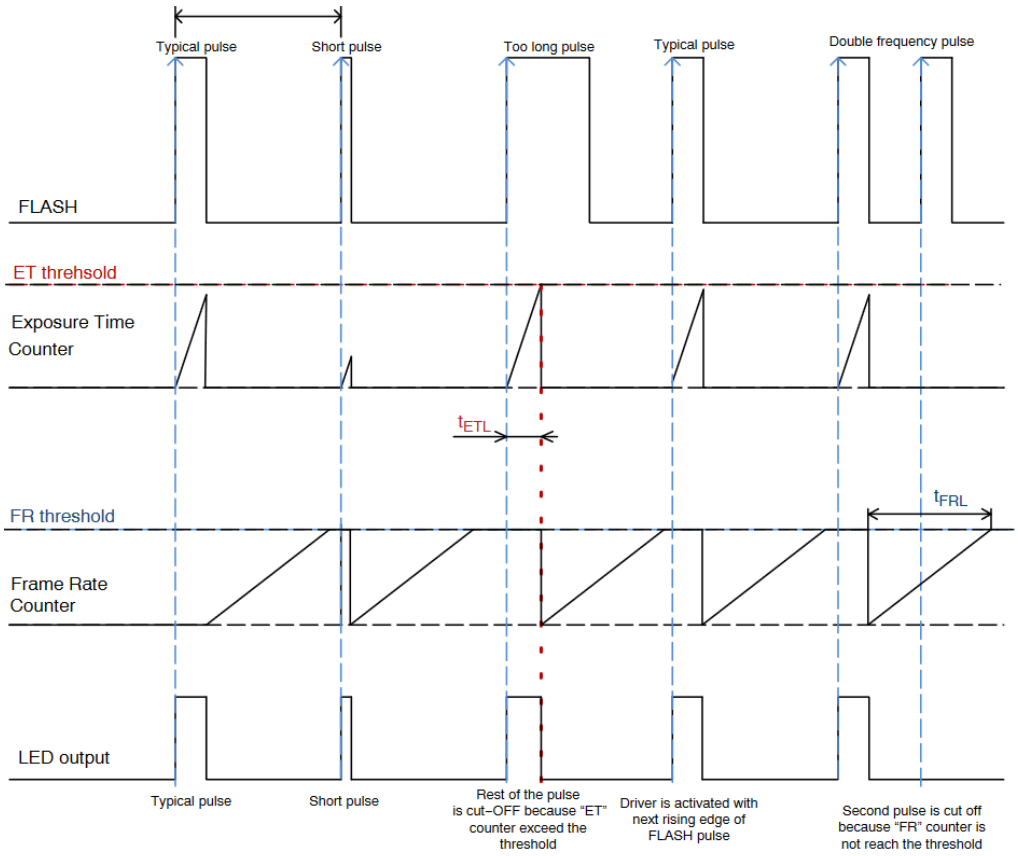

Figure 10. Operation of NCV7694 Eye−safety Protection Features

When the illuminated object is far from the NIR LEDs the reflected NIR light captured by the phototransistor T2 has very low intensity and T2 is cut−off.

The voltage supervisor NCV803SQ308D2T1G V_{CC} is biased from V_{PU} = 5 V through the resistor R_{PU} = 10 kΩ. The NCV803 supply current is 2.5 μA max. across T_A = −40°C to 105°C which creates 25 mV drop across R_{PU} and consequently V_{CC} for supply of the device is close to 5 V. As a result the /RST output is deactivated.

When the illuminated object approaches the NIR LEDs, T2 collector current starts to increase which causes the voltage drop across R_{PU} = 10 kΩ resistor to increase. Once V_{CC} drops below 3.08 V, the NCV803 /RST output is activated turning−off the LEDs. For V_{CC} to drop down to 3.08 V, T2 collector current of 190 μA is required.

Once the LEDs are turned−off V_{CC} rises back to a voltage of ~5 V. Due to an internal NCV803 reset delay /RST output remains in the logic low state for t_{RP} = 20−66 ms after V_{CC}~5 V is restored as shown on Figure 11.

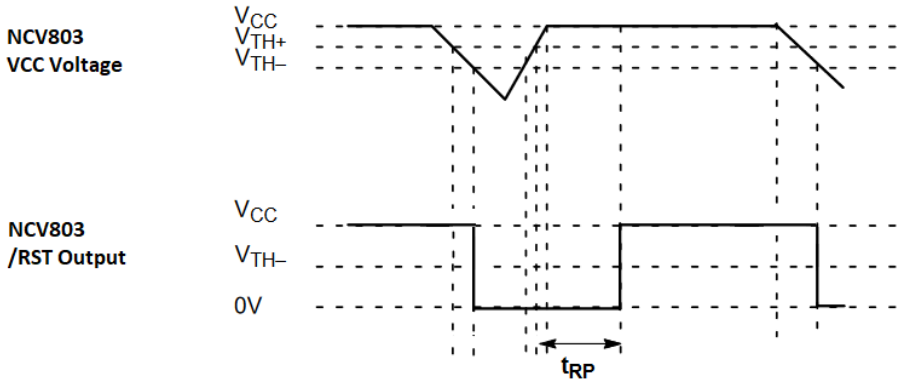

Figure 11. NCV803 Voltage Detector Operation

Programming the LED Current Level

The following equation can be used to set the nominal NIR LED current level:

$$I_{LED} = \frac{V_{SNS}}{R_{SNS}} \quad \text{(eq. 7)}$$

where:

I_{LED} – LED current (A)

V_{SNS} – 0.3 (V)
(V_{SNS} I is an internal NCV7694 voltage reference value. The reference has ±10% tolerance across operating junction temperature and process variation)

R_{SNS} – LED current sense resistor value (Ω).

In this design R_{SNS} = 75 mΩ was selected to supply the LEDs with a current of 4 A. It is worth highlighting that the NCV7694 has an internal diagnostic function which helps to identify and flag if an open or short across R_{SNS} is present.

In some cases, it may be necessary to adjust the LED current level in the application.

I.e. LED current adjustment may be needed in cases when reduction of LED pulse width is not feasible to implement. LED current adjustment may also help to save power by limiting the LED intensity during an optimal lighting conditions. i.e. a very bright sun light can negatively affect the quality of the captured images. In such cases, increasing of the NIR LED intensity could help to achieve higher quality images. During the night, when no or very limited sun light interference is present the NIR LEDs could operate with less intensity to reduce power losses.

This reference design doesn't include the LED current level adjustment functionality. Such a feature is, however, feasible to implement with NCV7694. Figure 12. shows how an external buffered Digital−to−Analog Converter (DAC) output can be connected to NCV7694 to adjust the LED current level.

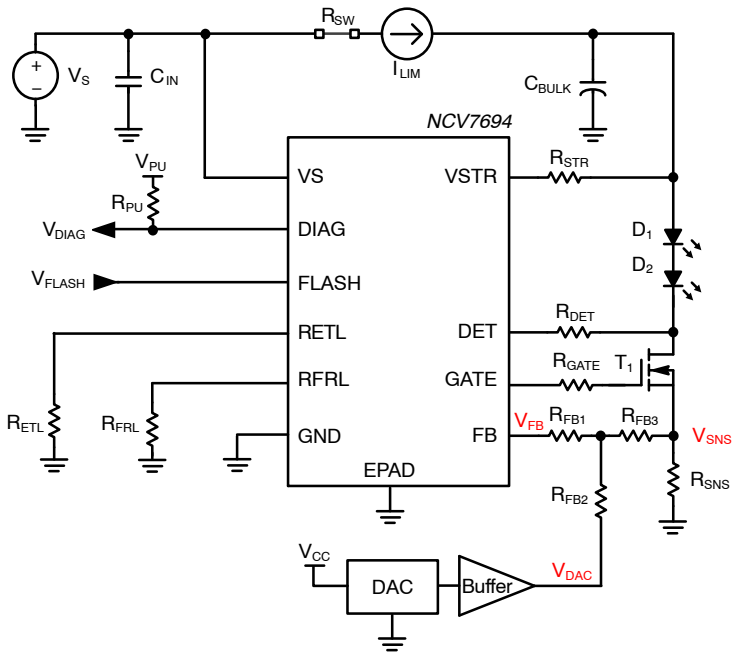

Figure 12. LED Current Level Adjustment through an External Digital−to−Analog Converter

Equations (8), (9) and (10) can be used to determine the component values needed to adjust the LED current in a specified range:

$$V_{SNS(MAX)} = \frac{V_{FB} \cdot I_{LED(MAX)} \cdot V_{DAC(MAX)}}{I_{LED(MAX)} [V_{DAC(MAX)} - V_{FB}] + I_{LED(MIN)} \cdot V_{FB}} \quad \text{(eq. 8)}$$

$$\frac{R_{FB3}}{R_{FB2}} = \frac{V_{SNS(MAX)} - V_{FB}}{V_{FB} - V_{DAC(MIN)}} \quad \text{(eq. 9)}$$

$$R_{SNS} = \frac{V_{SNS(MAX)}}{I_{LED(MAX)}} \quad \text{(eq. 10)}$$

where:

$V_{SNS(MAX)}$ – Maximum voltage across R_{SNS} corresponding to the target maximum LED current (V)

R_{SNS} – Sense resistor value (Ω)

$I_{LED(MAX)}$ – Target maximum LED current (A)

$I_{LED(MIN)}$ – Target minimum LED current (A)

V_{FB} – NCV7694 FB pin voltage = 0.3 (V)

$V_{DAC(MIN)}$ – Minimum DAC voltage (V)

$V_{DAC(MAX)}$ – Maximum DAC voltage (V)

R_{FB3} – Feedback resistor (Ω) (it is recommended to set R_{FB3} in the range of 330 Ω to 1 kΩ)

R_{FB2} – Feedback resistor (Ω)

The example below shows how to design a circuit which allows to set the LED current in a range between 0.5 A and 4.0 A using a voltage source adjustable in the range from 0 V to 3.1 V:

V_{FB} = 0.3 V, $I_{LED(MAX)}$ = 4 A, $I_{LED(MIN)}$ = 0.5 A, $V_{DAC(MAX)}$ = 3.1 V, $V_{DAC(MIN)}$ = 0 V, R_{FB3} = 470 Ω

From Equation (8):

$$V_{SNS(MAX)} = 0.328\ V$$

From Equation (9):

$$\frac{R_{FB3}}{R_{FB2}} = 0.093$$

After substituting R_{FB3} = 470 Ω into Equation (9):

$$R_{FB2} = \frac{470\ \Omega}{0.093} = 5.05\ k\Omega$$

From Equation (10):

$$R_{SNS} = 82\ m\Omega$$

Finally, the complete LED current adjustment circuit looks as follows:

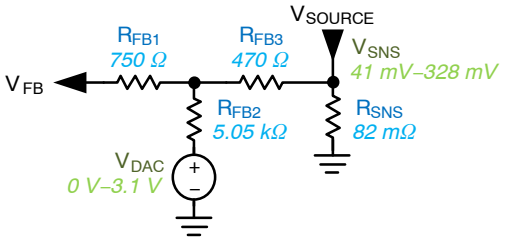

Figure 13. LED Current Adjustment Circuit

Design of the Input Current Limiting and High−side Protection Switch

To limit the hold−up capacitor charging current and provide a means to disconnect V_S from V_{BULK} during a fault event, the current limit switch, FPF2895V is used in the reference design. FPF2895V is an AEC−Q100 qualified intelligent high−side switch which offers the following features:

- Input to output adjustable current limiting
- Output to input current blocking
- Fixed undervoltage and adjustable overvoltage
- Overtemperature shutdown
- Fault output flag
- Configurable behavior upon tripping of the current limit

The very good dynamic behavior of the FPF2895V current limit loop assures that there are no significant input current overshoots when entering the current limit operation. This was verified during the device evaluation covered in Section Evaluation Results.

Figure 14 shows the actual implementation of FPF2895V in the reference design:

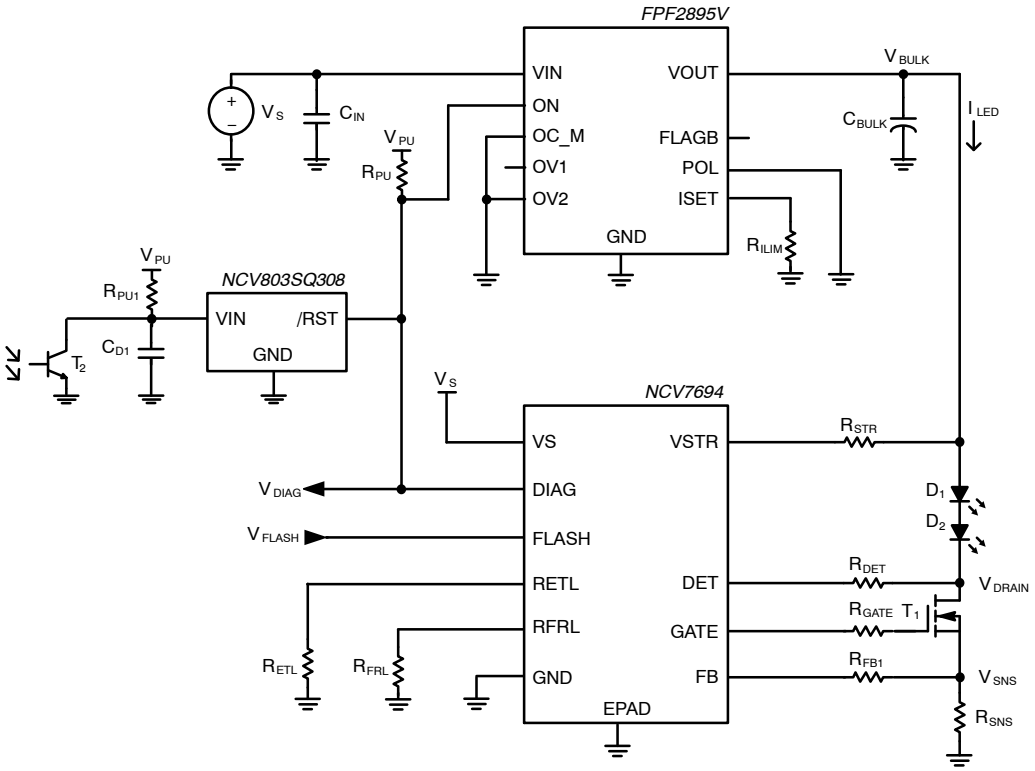

Figure 14. LED Driver with FPF2895V Current Limit and High−side Protection Switch

Resistor R_{ILIM} connected to pin I_{SET} of FPF2895V is used to set the current limit (C_{BULK} charging current) according to equation:

$$R_{ILIM} = \frac{4448.6}{I_{LIM}} \quad \text{(eq. 11)}$$

where:

I_{LIM} − target current limit value (mA)

R_{ILIM} − required current limit value (kΩ)

In the design example a 8.87 kΩ 1% R_{ILIM} resistor was used, which corresponds to a current limit of I_{LIM} = 501.5 mA (typ.). FPF2895V supports 15% current limit accuracy across −40°C to 105°C ambient temperature for an over−current limit range of 500 mA to 2 A.

Pin OC_M of FPF2895V is used to set the device behavior when in current limit. Pulling this pin low will cause the device to function as a constant current source. Pulling OC_M high enabled an auto−restart mode.

Pins OV1 and OV2 of FPF2895V allow to set the overvoltage lockout (OVLO) threshold according to Table 2:

Table 2. SUPPORTED FPF2895V OVLO LEVELS

OV1	OV2	OVLO Level
Low	Low	23 V (typ.)
Low	High (Floating)	10 V (typ.)
High (Floating)	Low	16.8 V (typ.)
High (Floating)	High (Floating)	5.95 V (typ.)

As the nominal supply voltage V_S in the application example is 12 V and the C_{BULK} rating is 16 V, the OVLO level was set to 16.8 V (typ.). Across process spread and ambient temperature variation between −40°C and 105°C, the OVLO level can range between 16.3 V and 17.1 V.

The FPF2895V POL pin is used to set the ON pin polarity. ON input is a low voltage logic input used to disable or enable the device output. In the reference design a positive polarity was set. As a result, the device will be turned−on whenever ON pin voltage is brought above 1.2 V.

ON input is pulled−up to an onboard 5 V LDO output, as shown in Figure 14. The FPF2895V ON input is pulled down by two sources:

1. NCV7694 LED driver /DIAG pin (open−drain, active low output)
   The /DIAG output is activated as soon as NCV7694 detects any of the following faults:
   - LED anode to cathode open circuit
   - LED anode to cathode short
   - LED cathode short to ground
   - Flash input being too long or too frequent
   - VS undervoltage or VS Overvoltage
   - Overtemperature
2. NCV803 Light Sensor Comparator /RST pin (open−drain, active low output)
   As the illuminated object gets closer to the LEDs, the T2 collector current increases creating a larger voltage drop across R_{PU1} and eventually the NCV803 /RST output is pulled low.

When selecting the current limiter, it is important to verify that the selected IC can meet the required power dissipation profile in the target system. To complete this verification a SPICE simulation was set up according to Figure 15.

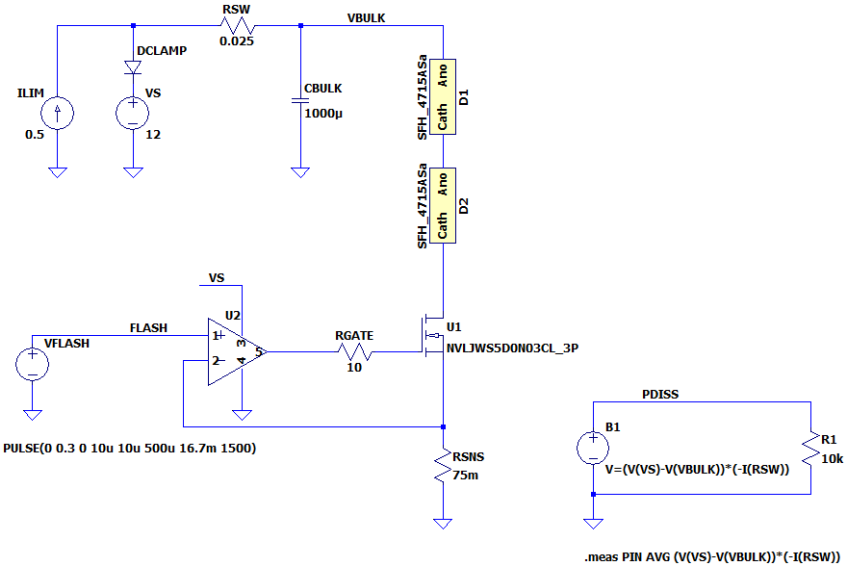

Figure 15. LED Current Adjustment Circuit

The resulting high−side switch power dissipation profile can be seen on Figure 16. The power dissipation has a triangular shape with peak power reaching 0.9 W at the end of the 500 μs LED on pulse. The average power dissipation is 105 mW. Based on this thermal analysis it was confirmed that at $T_{A(MAX)}$ = 85°C the device maximum junction temperature $T_{J(MAX)}$ will stay below 125°C during operation.

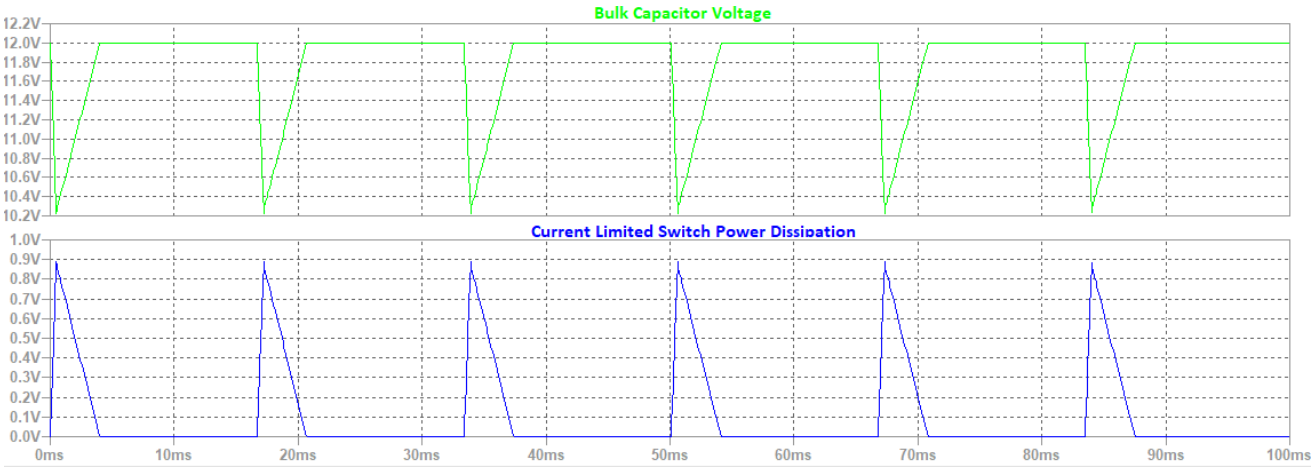

Figure 16. LED Current Adjustment Circuit

REFERENCE DESIGN SCHEMATIC

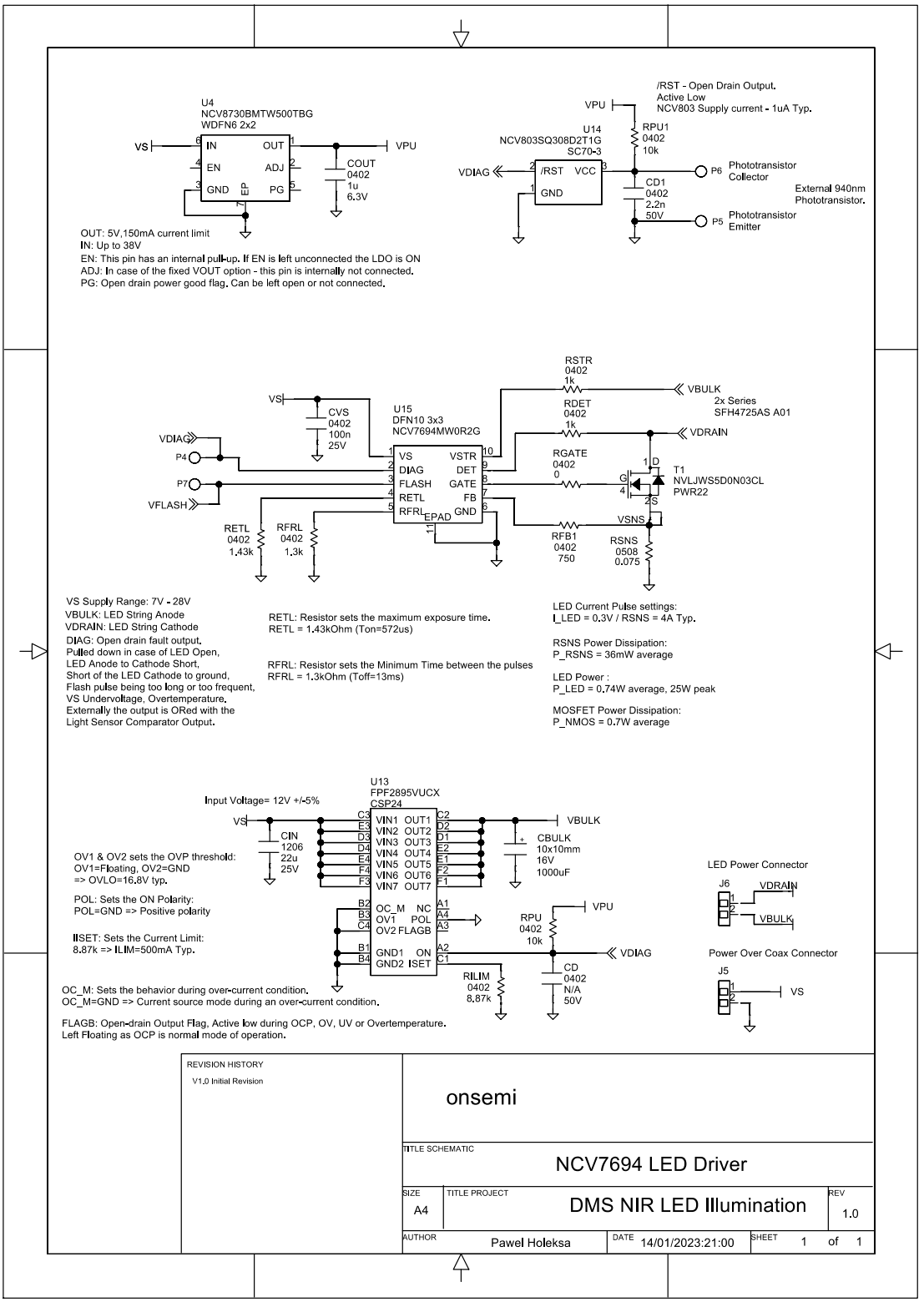

Figure 17. Schematic of DMS LED Driver Reference Design

REFERENCE DESIGN LAYOUT

The NIR LED driver reference design is based on a 15x15 mm 4−layer FR−4 PCB. The top layer contains all the components besides the hold−up capacitor which is placed on the bottom layer. Copper polygons are used on the bottom side to minimize the effects of parasitic inductance when turning−on and off the LED current. The signal traces are routed on the top and inner2 layers. Inner1 layer is entirely covered by a GND copper plane.

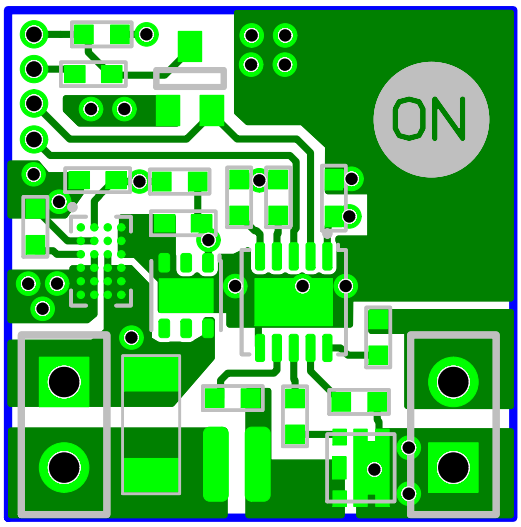

Figure 18. Top Layer

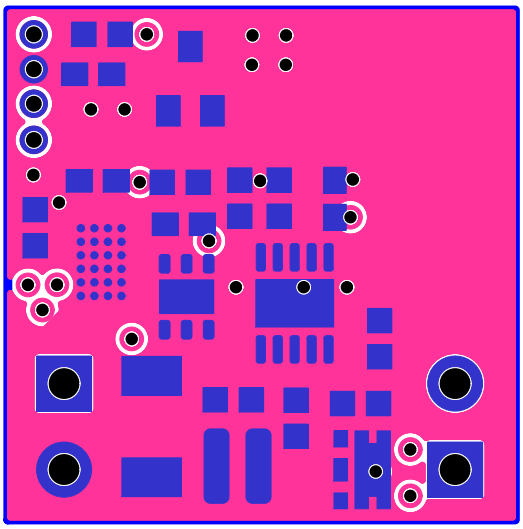

Figure 19. Inner1 Layer

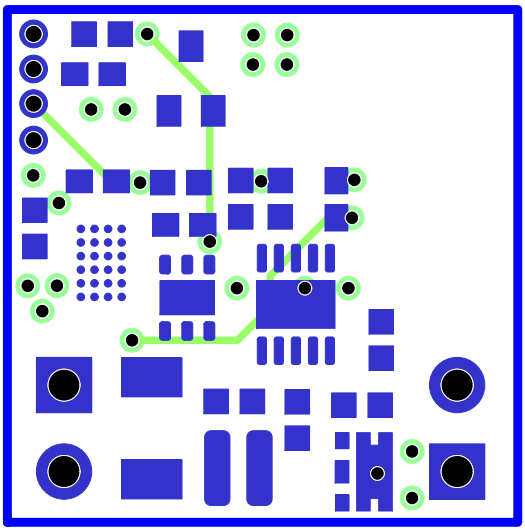

Figure 20. Inner2 Layer

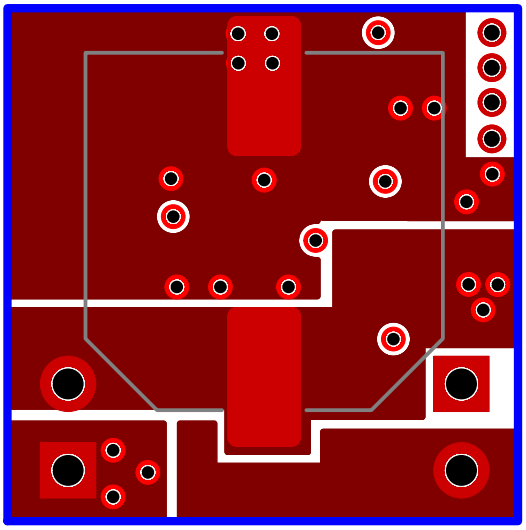

Figure 21. Bottom Layer

REFERENCE DESIGN BILL OF MATERIALS

Table 3. BILL OF MATERIALS

Reference Designator	QTY	Part Number	Supplier	Package	Description	Value
CD1	1	UMF105B7222KVHF	Taiyo Yuden	0402	MLCC X7R 2.2 nF 10%, 50 V 0402	2.2 nF
CD	1	N/A	N/A	0402	Part not populated	2.2 nF
CVS	1	C0402C104K3RACTU	Kemet	0402	MLCC X7R 100 nF 10%, 25 V 0402	100 nF
CIN	1	GRM31CC71E226ME15L	Murata	1206	MLCC X7S 22 μF 20%, 25 V 1206	22 μF
COUT	1	GRM155R70J105MA12D	Murata	0402	MLCC X7R 1 μF 20%, 6.3 V 0402	1 μF
P4−P7	4	5002	Keystone	Thru−Hole	Miniature testpoint, 1 mm, White	N/A
RPU, RPU1	2	AC0402FR−0710KL	Yageo	0402	Resistor 10 kΩ 62.5 mW 1%, AEC−Q200	10.0 kΩ
RFB1	1	AC0402FR−07750RL	Yageo	0402	Resistor 750 Ω 62.5 mW 1%, AEC−Q200	750 Ω
RGATE	1	AC0402FR−070RL	Yageo	0402	Resistor 0 Ω 62.5 mW 1%, AEC−Q200	0 Ω
RILIM	1	AC0402FR−078K87L	Yageo	0402	Resistor 8.87 kΩ 62.5 mW 1%, AEC−Q200	8.87 kΩ
RDET, RSTR	2	AC0402FR−071KL	Yageo	0402	Resistor 1.0 kΩ 62.5 mW 1%, AEC−Q200	1.0 kΩ
RFRL	1	AC0402FR−071K3L	Yageo	0402	Resistor 1.3 kΩ 62.5 mW 1%, AEC−Q200	1.3 kΩ
RETL	1	ERJ−2RKF1431X	Panasonic	0402	Resistor 1.43 kΩ 62.5 mW 1%, AEC−Q200	1.43 kΩ
RSNS	1	LTR10EVHFSR075	Rohm	0508	Current Sense Resistor 75 mΩ 1%, AEC−Q200	0.075 Ω
T1	1	NVLJWS5D0N03CL	**onsemi**	PWR22 2x2	Logic Level Power NMOS, 30 V 4.2 mΩ	N/A
U4	1	NCV8730BMTW500TBG	**onsemi**	WDFN6 2x2	LDO regulator, Ultra−Low Iq, 5 V Vout	N/A
CBULK	1	PCR1C102MCL1GS	Nichicon	10x10 mm	Aluminum Polymer Capacitor 16 V 1000 μF 20% 13 mΩ, AEC−Q200	1000 μF
U13	1	FPF2895VUCX	**onsemi**	CSP24	Current Limit Switch with OVP, 28 V/5 A	N/A
U14	1	NCV803SQ308D2T1G	**onsemi**	SC70−3	Voltage Detector, Ultra−Low Iq	N/A
U15	1	NCV7694MW0R2G	**onsemi**	DFN10 3x3	Safety Controller for NIR LED Illumination	N/A

Evaluation of the NCV7694 NIR LED driver reference design

Evaluation Platform Description

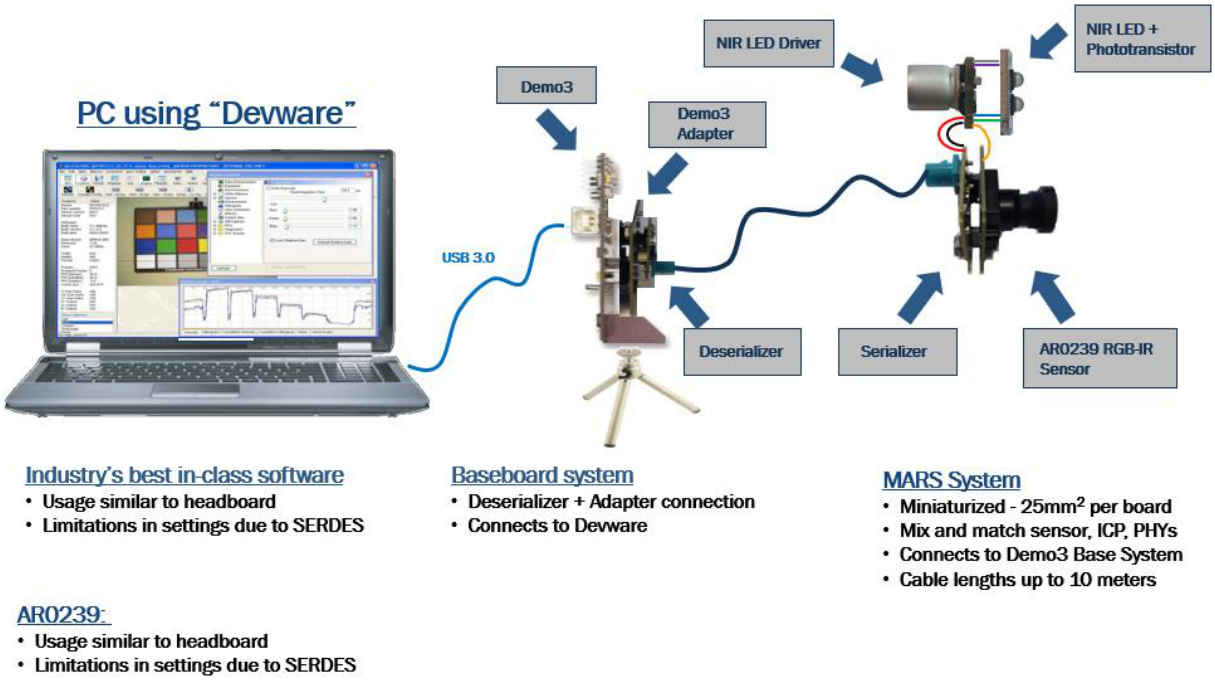

Figure 22. DMS NIR LED Driver Evaluation Setup

Figure 22 shows **onsemi**'s platform used to evaluate the NCV7694 NIR LED driver reference design in a POC based camera system. Evaluation was done based on a AR0239 RGB−IR image sensor and the NCV7694 NIR LED driver reference design both powered by a regulated 12 V POC. The NCV7694 LED driver FLASH input was connected to the FLASH output of the AR0239 RGB−IR sensor and the NCV7694 NIR LED driver /DIAG output was connected to a serializer GPIO pin. **onsemi**'s Devware software was used to configure the image sensor to stream, capture the image data and investigate the image quality. The 12 V POC power supply was powered by a 5 V USB port of the computer through a 5 V to 12 V boost converter, which is part of the Deserializer board. If needed, the Deserializer board allows disconnection from the onboard boost converter and connection to an external POC power supply.

The following evaluation has been performed on the NCV7694 reference design:

- Evaluation of the eye−safety protection features
- Evaluation of the current limit functionality
- Evaluation of V_{BULK} and I_{LED} and comparison with the calculated values from Section Step−by−step Design Guide

Evaluation Results

Figure 23 shows the typical operating waveforms of the NCV7694 based LED Driver. The FLASH signal is being activated every 16.67 ms which corresponds to an image sensor frame rate of 60 fps. The duration of the flash signal is set to 500 μs. As no fault is present, V_{DIAG} is pulled−up to 5 V. During the LED on−time V_{SNS} is being regulated to 0.3 V and V_{BULK} drops linearly as C_{BULK} is being discharged with a constant current. Once V_{FLASH} is turned−off, V_{SNS} drops to 0 V and V_{BULK} recovers linearly to 12 V.

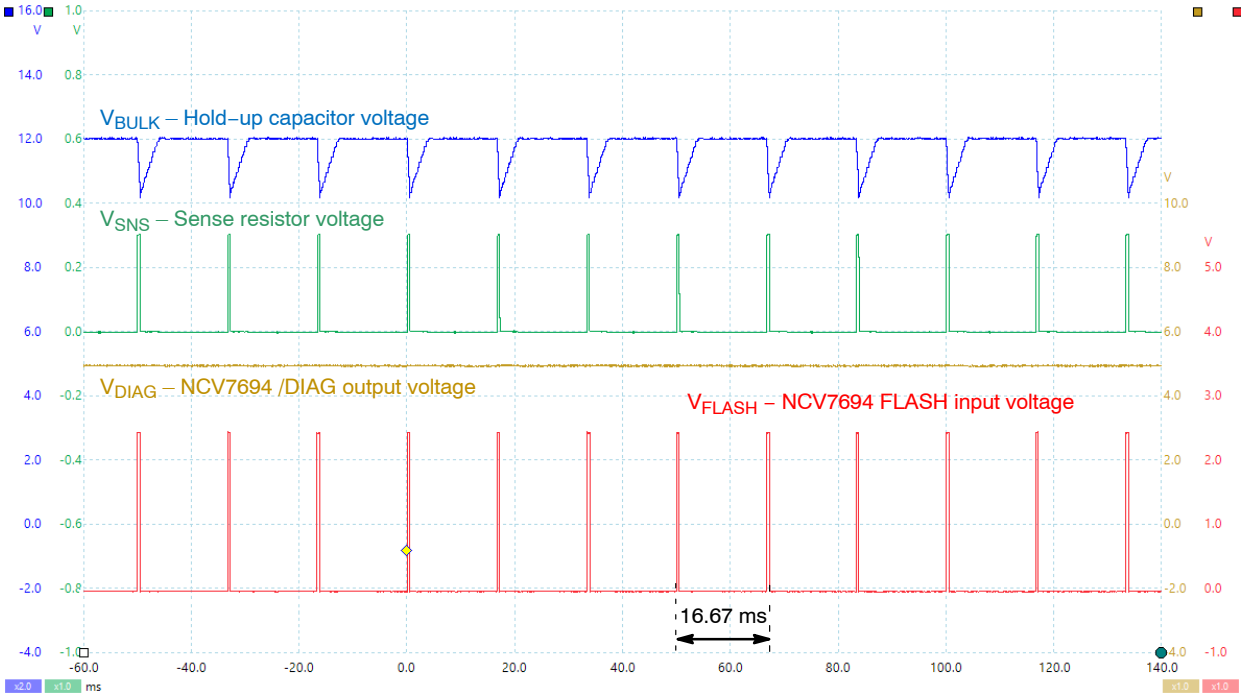

Figure 23. NCV7694 LED Driver – Typical Operating Waveforms

Figure 24 shows the typical operating waveforms in more detail. During the LED on−time T_{ON} = 500 μs, V_{BULK} drops by 1.82 V. A quick verification based on Equation 4 gives C_{BULK} = 960 μF which is in−line with the actual C_{BULK} value. During T_{CHARGE} the hold−up capacitor is charged with a 500 mA constant current assured by FPF2895V the current limitation. Measured charging time of 3.51 ms is in−line with the previous calculations.

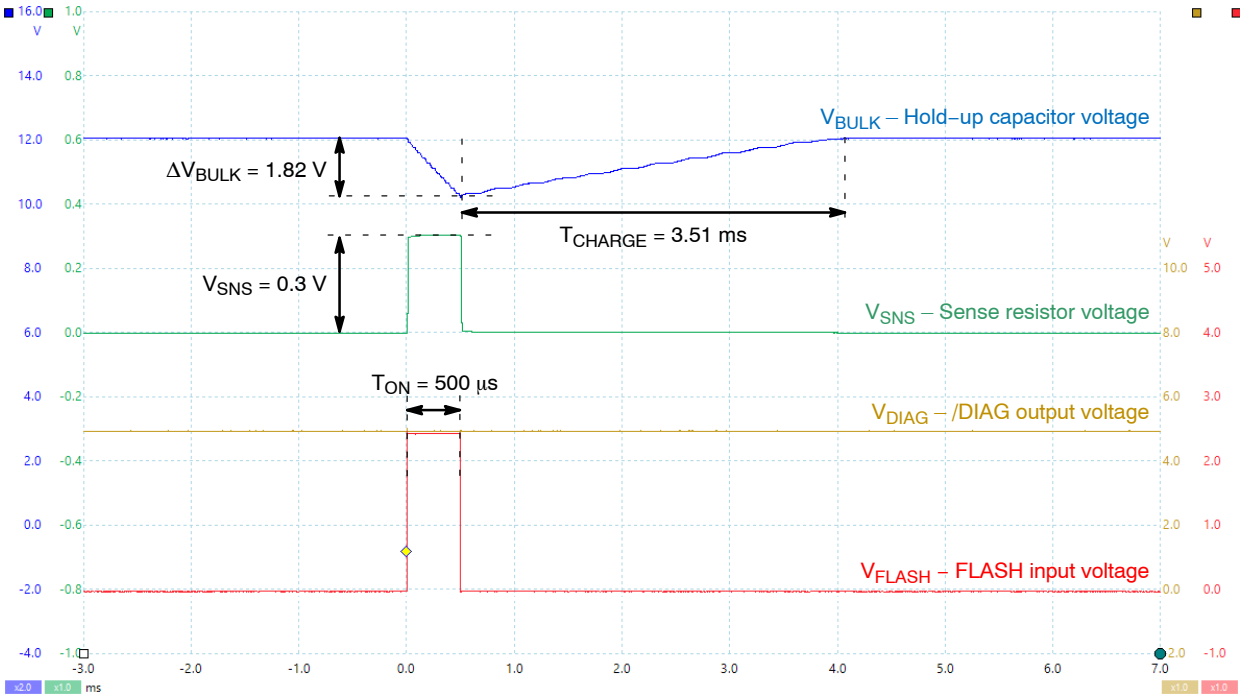

Figure 24. NCV7694 LED Driver – Typical Operating Waveforms

Figure 25 shows the T1 gate voltage as well as the V_{SNS} signal after enabling the FLASH input. T1 gate starts to rise ~1.8 μs after applying of V_{FLASH}. It takes *~6.4 μs* for T1 gate to exceed the threshold voltage and start to regulate drain current. The LED current increases smoothly without any overshoot which indicates good feedback loop stability.

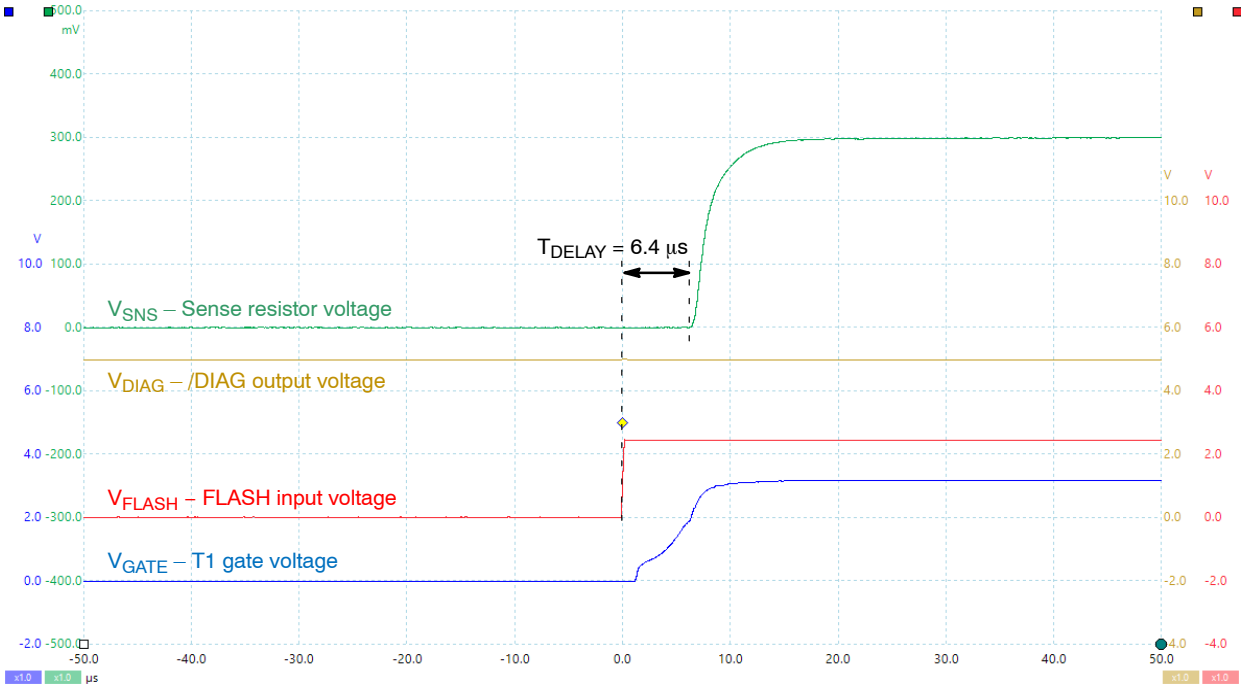

Figure 25. LED Current Turn−on – Detailed View

Figure 26 shows T1 gate voltage as well as V_{SNS} signal after disabling the FLASH input. T1 gate starts to decrease instantly after de−asserting of V_{FLASH} signal. It takes ~20.5 μs for V_{SNS} to decrease close to 0 V.

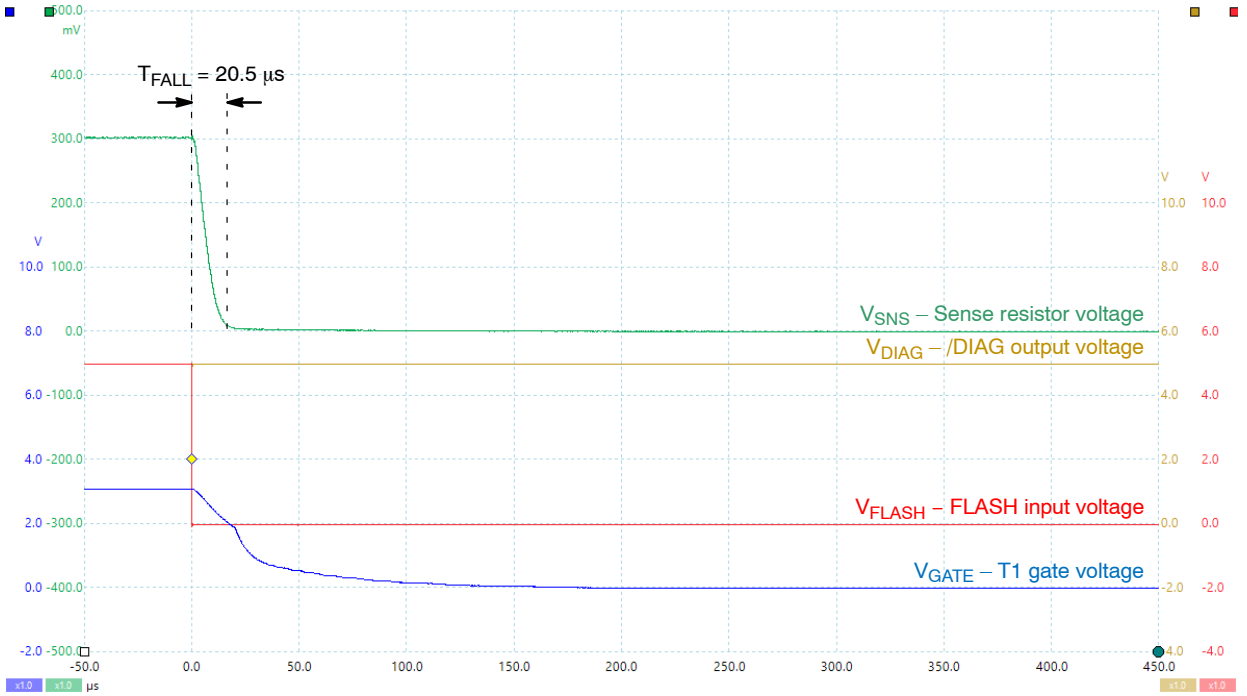

Figure 26. LED Current Turn−off – Detailed View

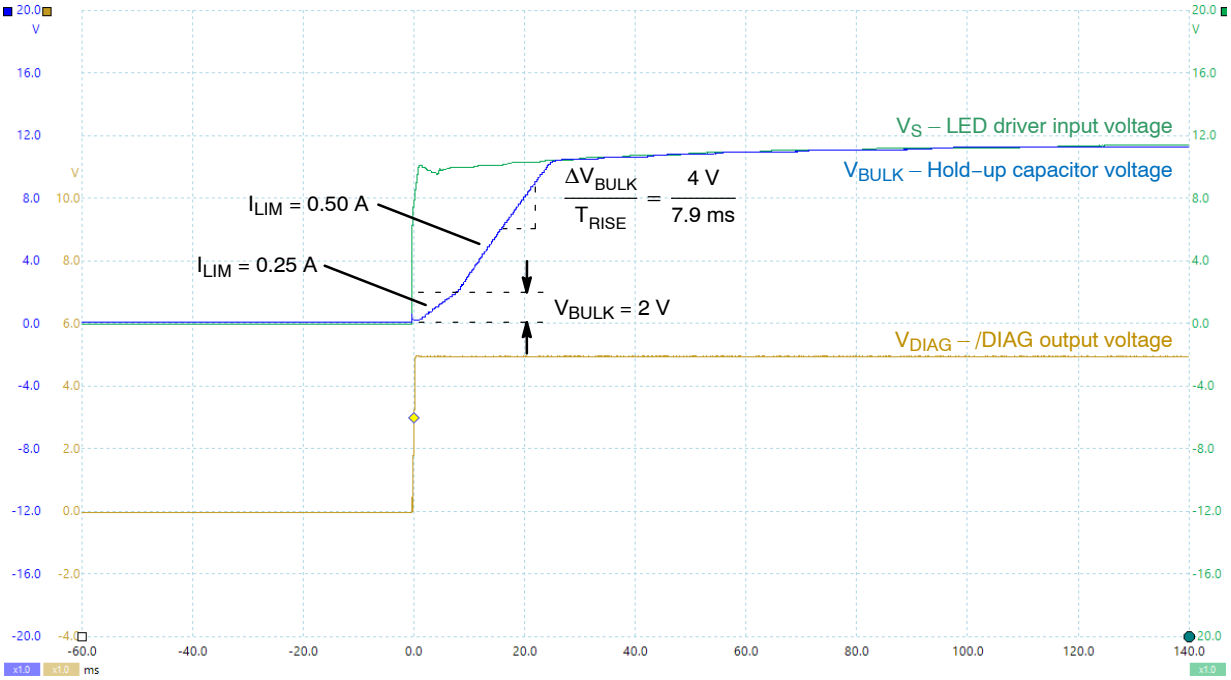

Figure 27. Start−up of the LED Driver

Figure 27 shows the LED driver start−up waveforms. Once the V_S input voltage is applied initially, V_{BULK} is being charged with a constant current of 250 mA. This is because of an FPF2895V foldback current limit functionality. Once V_{BULK} exceeds 2 V, the FPF2895V current limit is increased to 500 mA. The overall V_{BULK} charging time from 0 V to 12 V takes ~28 ms. V_{DIAG} is pulled−up to V_{PU} through 10 kΩ, therefore V_{DIAG} = 5 V shortly after start−up.

Figure 28 shows the T1 MOSFET drain and source voltage as well as T1 Power dissipation. During typical operating conditions at room temperature V_{DRAIN} drops down to 4 V. This assures an additional margin for worst case conditions. The maximum T1 power dissipation is 22.5 W while the average power dissipation is 585 mW. The measured value is slightly lower compared to the calculated value in section MOSFET Selection. However, this is according to the expectation as 706 mW calculated in section MOSFET Selection was assuming worst case conditions.

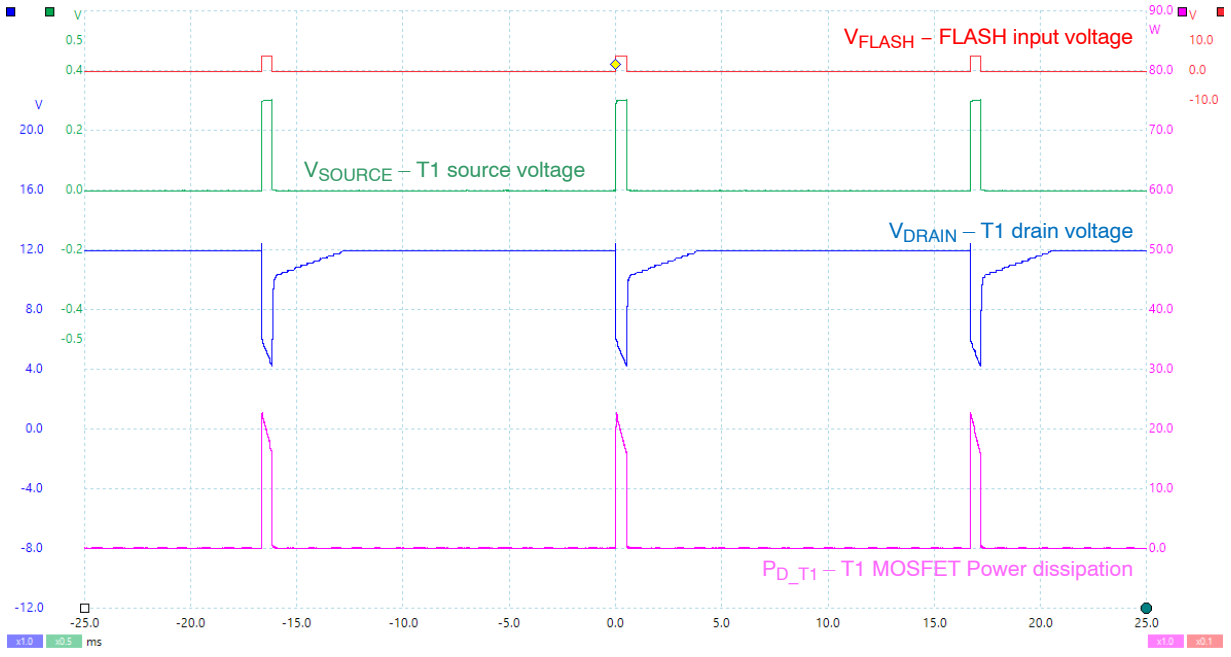

Figure 28. T1 MOSFET Waveforms

Figure 29 shows the LED voltages and power dissipation. The LED power dissipation was determined to be 25 W peak and 735 mW in average. The typical forward voltage drop across 2 series LEDs at 4 A was measured to be is 6.2 V.

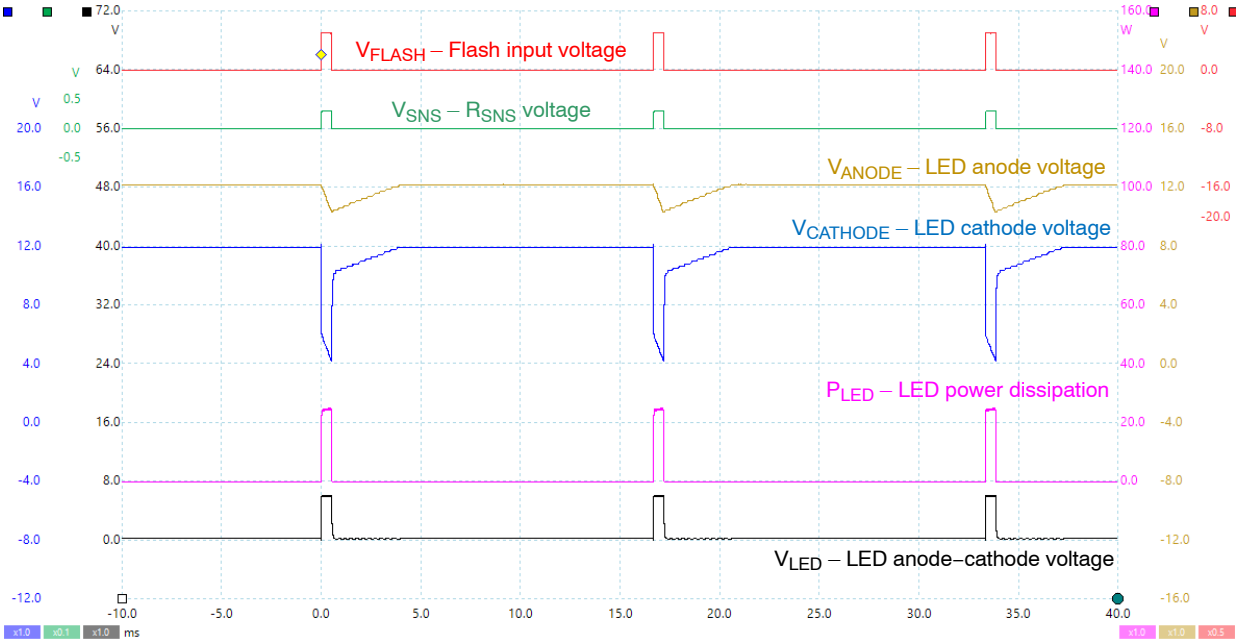

Figure 29. NIR LED Waveforms

Figure 30 shows operation of the LED turn−on time limitation. Once V_{FLASH} exceeds the programmed LED turn−on time limit of 570 μs, V_{DIAG} goes low to indicate a fault condition. T1 and FPF2895V are both disabled. Once the prolonged V_{FLASH} pulse is disabled, the system returns to normal operation. V_{DIAG} increases to 5 V and FPF2895V turns−on. Due to an internal turn−on delay implemented in the FPF2895V it takes ~2.8 ms for the device to restart charging of V_{BULK}.

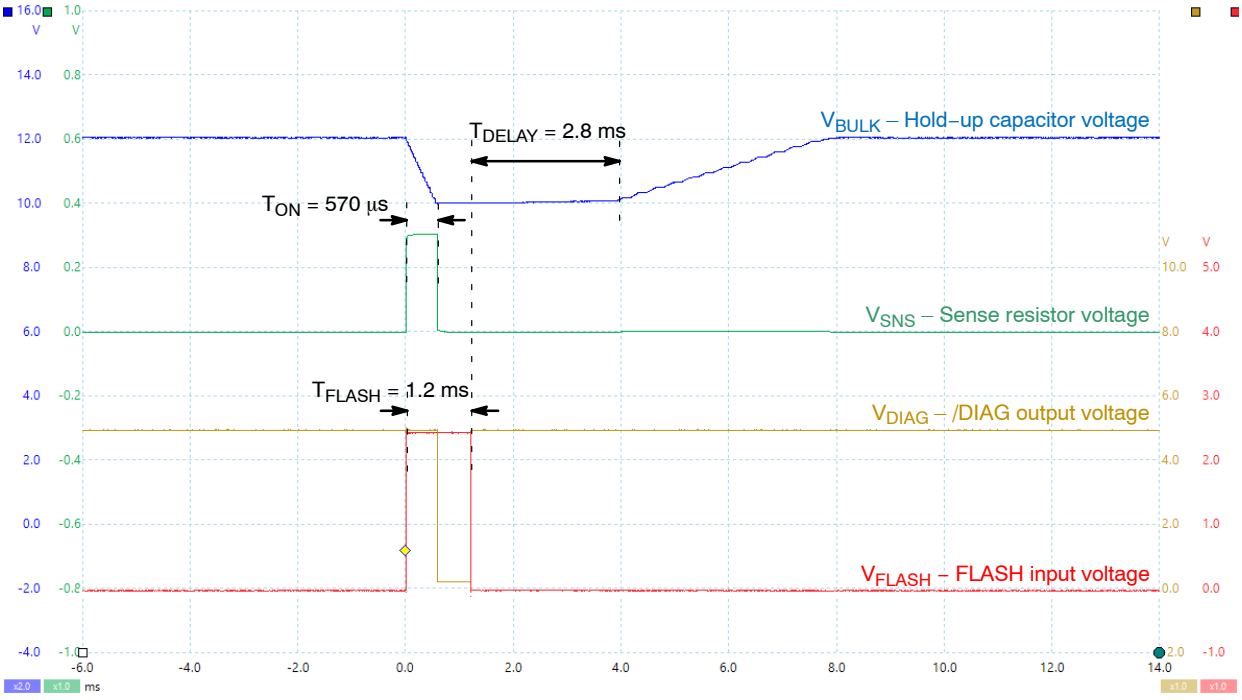

Figure 30. Operation of LED Maximum Turn−on Time Limitation

Figure 31 shows operation of LED maximum turn−on time limitation in more details. T1 gate is pulled low immediately after V_{DIAG} is disabled. It takes ~20 μs for the LED current to drop from 4 A down to ~0 A.

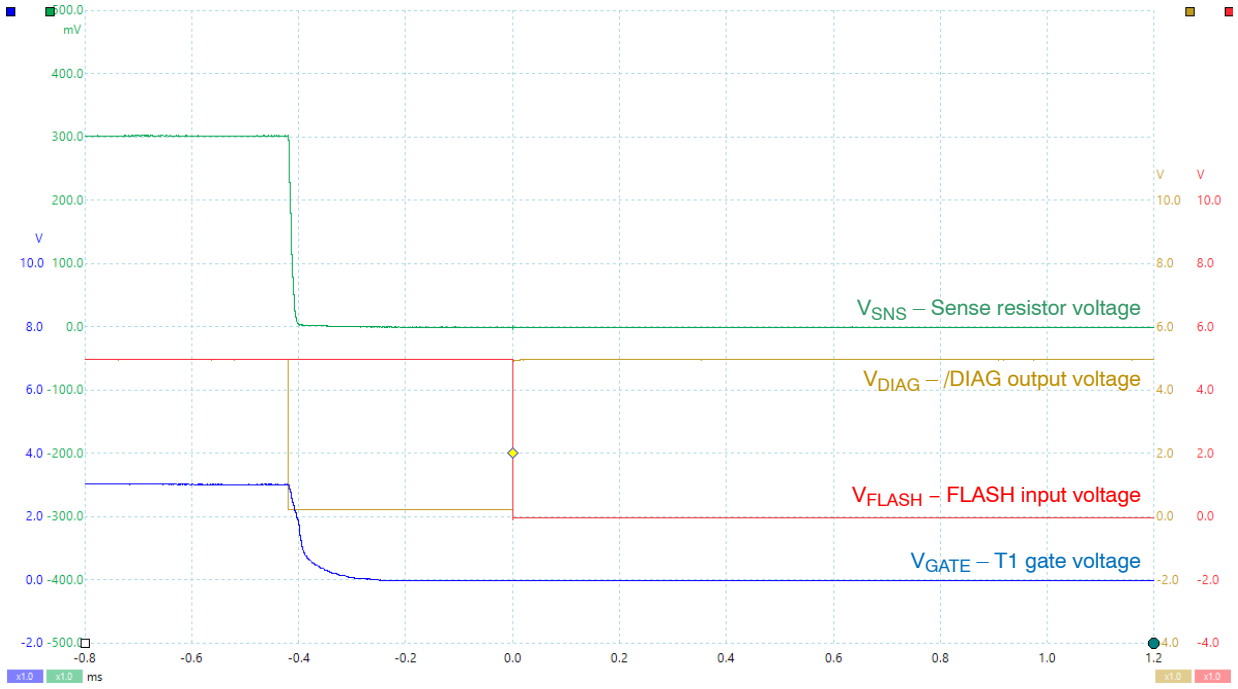

Figure 31. Operation of LED Maximum Turn−on Time Limitation – Detailed View

Figures 32 and 33 demonstrate operation of minimum LED turn−off time limitation for two different flash signal periods. In Figure 32 the FLASH signal period was set to 12.5 ms which corresponds to 80 Hz. The time between FLASH pulses in this case is 12 ms, which exceeds the programmed time of 13 ms. As a result, the LEDs are being activated every second FLASH input pulse, with a period of 25 ms (40 Hz). In Figure 33 the FLASH signal frequency was increased to 180 Hz, corresponding to a FLASH period of 5.55 ms. As a result, the actual LED turn−on frequency is divided by 3.

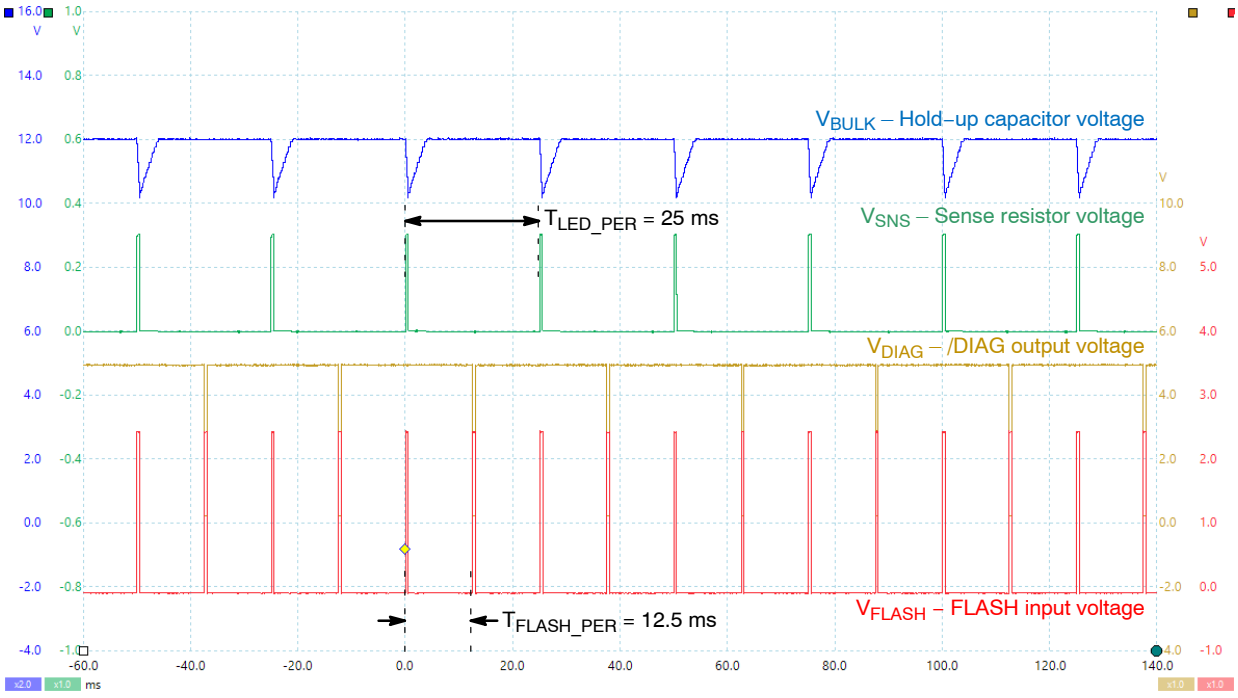

Figure 32. Operation of Minimum LED Turn−off Time Limitation

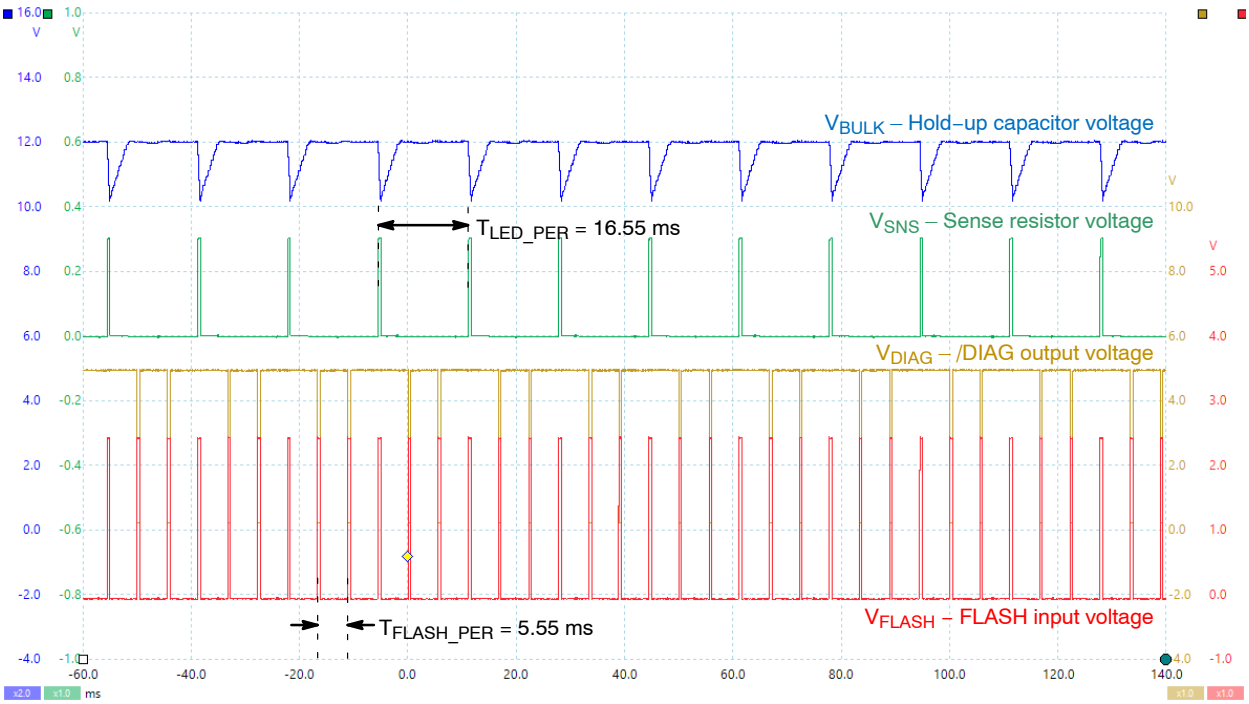

Figure 33. Operation of Minimum LED Turn−off Time Limitation

Figure 34 shows that there is a small delay between enabling of the FLASH input pulse and detecting an insufficiently short LED turn−off time fault.

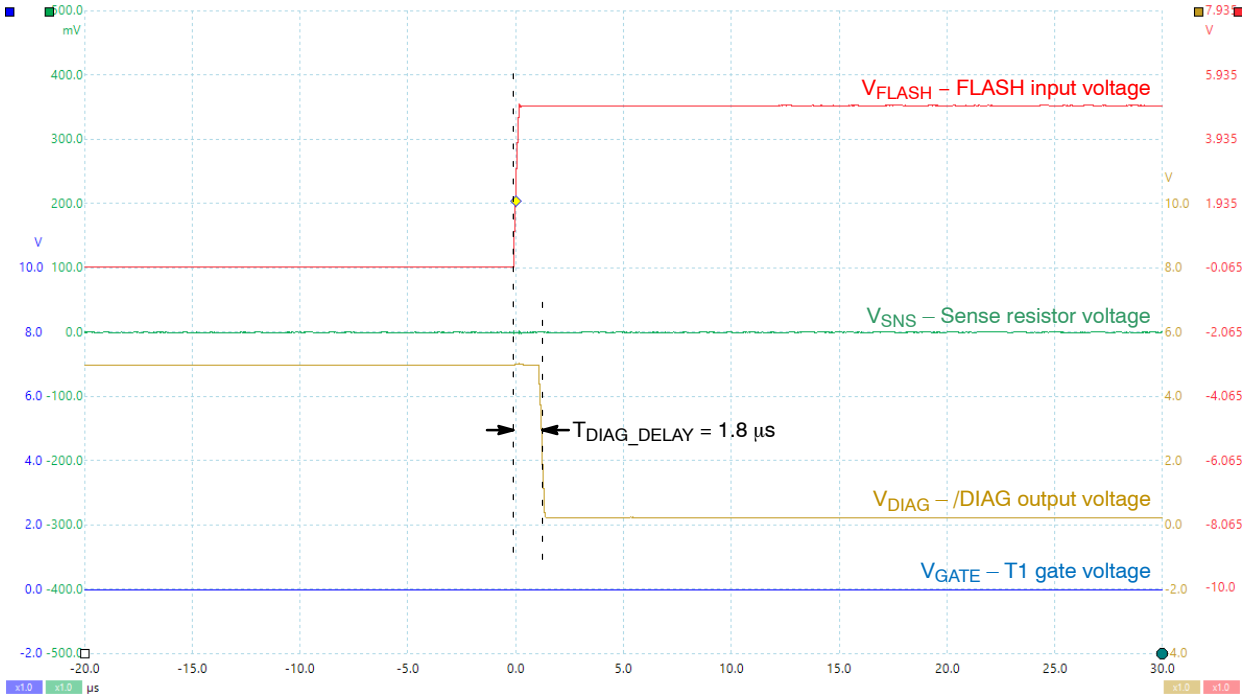

Figure 34. Operation of Minimum LED Turn−off Time Limitation – Detailed View

Figure 35 shows a condition where the FLASH input signal is being applied for too long a period and with a frequency that is too high. Both faults are correctly detected and handled by NCV7694.

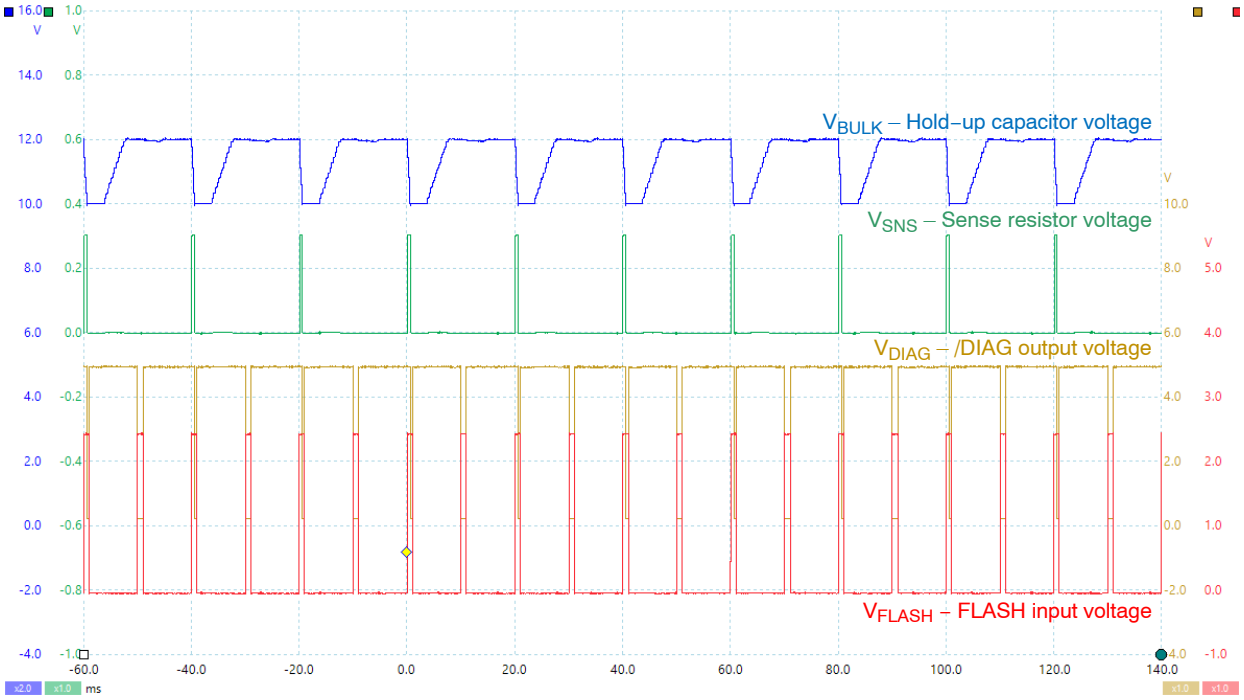

Figure 35. Operation of Minimum LED Turn−off Time and Maximum LED Turn−on Time Limitations

Figure 36 shows the driver operation during a LED anode−to−cathode short circuit condition. NCV7694 monitors the LED string anode−to−cathode voltage and reports a fault in case if this voltage drops below 1.22 V. V_{DIAG} is pulled low 30 μs after the FLASH input gets activated. During this condition MOSFET T1 is exposed to a higher−than−normal peak power dissipation, but it survives this test.

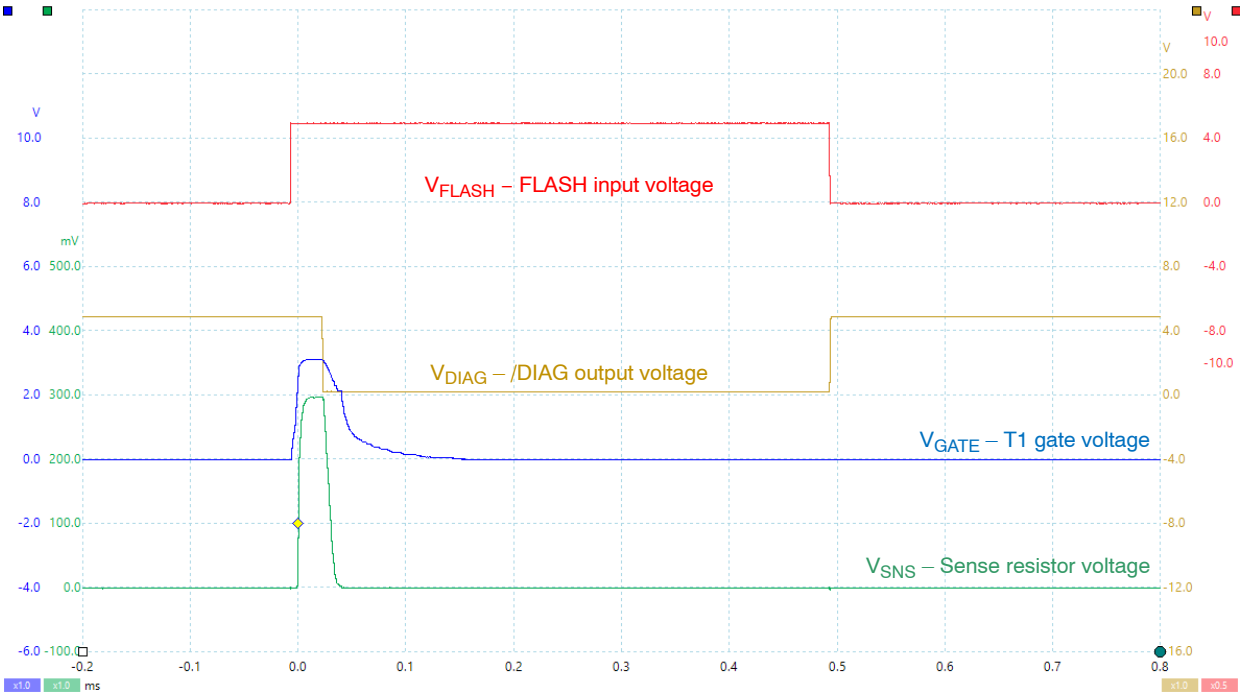

Figure 36. LED Driver Operation During LED Anode−to−Cathode Short

Figure 37 shows a condition where the T1 MOSFET drain is shorted to GND when the FLASH signal is disabled. Such condition leads to a rapid discharge of V_{BULK}. NCV7694 detects that the voltage at V_{DET} drops below 0.35 V and pulls−down V_{DIAG} to GND after 10 μs of blanking period. Once a FLASH signal is activated with T1 MOSFET drain shorted to GND, NCV7694 detects that V_{DET} < 0.35 V and V_{SNS} < 0.15 V which again leads to asserting of a fault and pulling−down V_{DIAG}. V_{DIAG} is pulled down after 10 μs or 22 μs depending on which fault is detected as first.

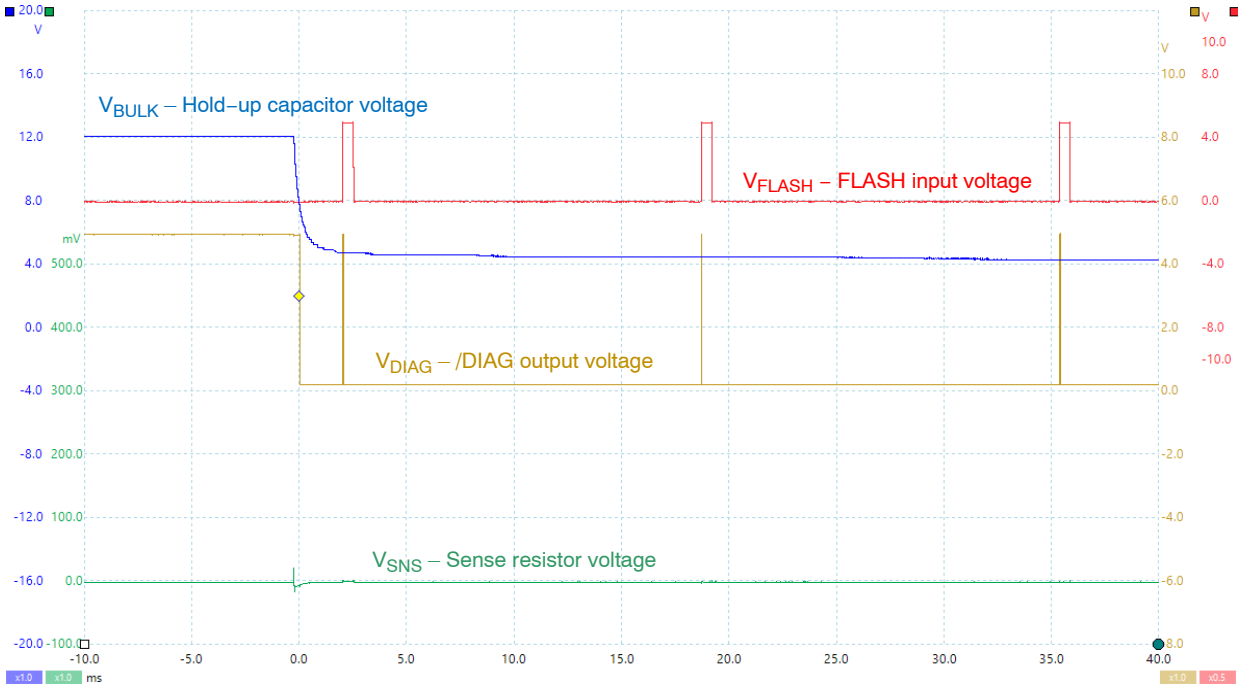

Figure 37. LED Driver Operation During T1 MOSFET Drain Short to Ground

Figure 38 demonstrates T1 V_{DS} short situation when V_{FLASH} is disabled. In this case a large current up to 20 A peak is drawn momentarily from C_{BULK}. The capacitor quickly discharges and as soon as V_{DET} drops below 0.35 V, V_{DIAG} pin goes low indicating a fault and disabling FPF2895V load switch. If the fault persists when V_{FLASH} is active, then V_{DIAG} is pulled down after 10 μs or 22 μs depending on which fault is detected first.

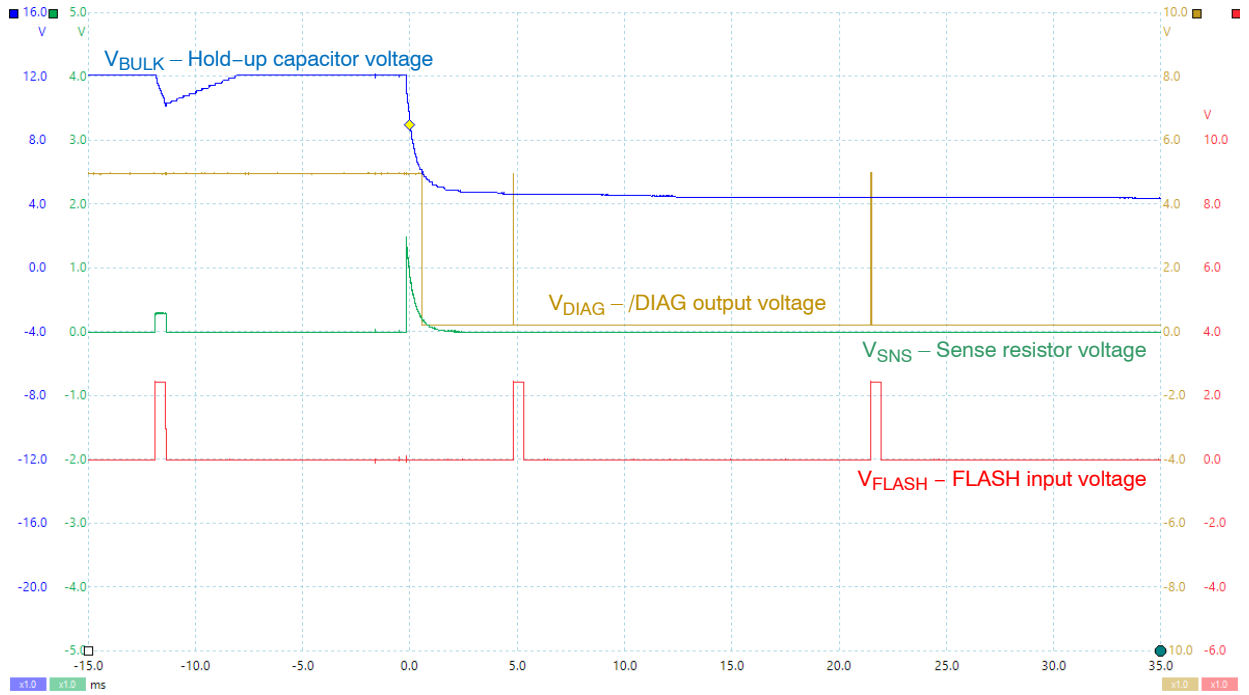

Figure 38. LED Driver Operation During T1 MOSFET V_{DS} Short

Figure 39 demonstrates operation of the LED driver input overvoltage protection. As soon as the LED driver input voltage V_S exceeds 16.8 V, the FPF2895V high−side switch becomes disabled which terminates charging of the hold−up capacitor V_{BULK}.

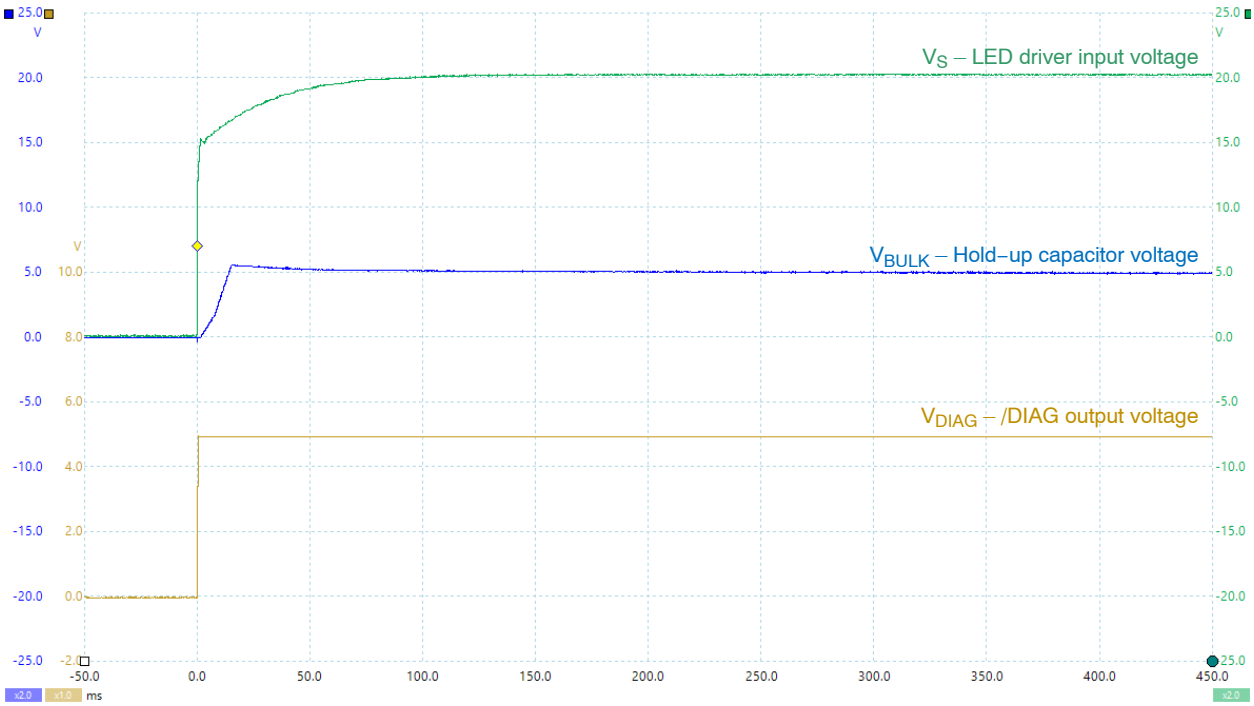

Figure 39. LED Driver Operation During Input Overvoltage Condition

CONCLUSIONS

This **onsemi** reference design details a complete solution for a NIR LED driver for driver and occupant monitoring applications. The design is based entirely on the following onsemi ICs:

- NCV7694 LED driver
- FPF2895V current limited high−side switch
- NCV803 voltage detector
- NCV8730 LDO

The described design features are an extensive set of protection and diagnostic mechanisms covering LED string open and short circuit protection, eye−safety protection, MOSFET short circuit protection, input current limit, input overvoltage protections. This reference design provides a step−by−step guide on the design of each of the different building blocks:

- Current limit
- Over−voltage protection
- Hold−up capacitor
- Eye−safety protection
- Power MOSFET
- LED current regulation loop

The design was evaluated during normal operation and during various fault cases covered in section Evaluation Results.

REFERENCES

[1] G. Breglio, F. Frisina, A. Magri, and P. Spirito, “Electro−Thermal Instability in Low Voltage Power MOS: Experimental Characterization,” IEEE Proceedings ISPSD 1999, Toronto, p233

ADDITIONAL INFORMATION

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